

Abstract

This paper explores the feasibility of constructing an autonomous sensor array on a standard silicon wafer. Such a sensor-wafer would include integrated electronics, power, and communications, and would be capable of being placed into a standard production run. During the processing of the sensor-wafer, various process parameters would be measured and recorded. There are several uses for such a sensor wafer, including equipment characterization and design, process calibration, and equipment problem diagnosis. In this paper, various sensor architectures, power supplies, communications methods, and isolation techniques are discussed, and particular choices are made. Three proof-of-concept designs utilizing a four-point probe film-thickness measurement scheme are discussed, and test results are reviewed for each design.

***In-Situ* Etch Rate Sensor Arrays for Plasma Etch Processes**

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Chapter 1

Introduction

Over the past few years, the semiconductor processing industry has undergone a paradigm shift from *ex-situ* metrology to in-line metrology. Wafer measurement equipment has been moved, where possible, from stand-alone measurement stations to integrated measurement systems on or near the processing equipment. The benefits of this shift have been significant. Among the advantages of in line metrology are improved process monitoring, reduced product variance, and higher throughput. By placing the sensors on the equipment, *every* wafer is examined, as opposed to just a fraction, as is the case with standalone metrology stations. Because much more data is available, process fluctuations and trends can be much better monitored and recorded. Also, because the data is taken more frequently, adjustments to the process can be made more frequently, so product variance can be reduced. Finally, by measuring all of the wafers in-line and allowing them to continue instead of removing selected wafers for metrology, more production wafers can reach process completion, improving throughput.

While the benefits of in-line metrology are numerous, the money and time spent to integrate metrology stations onto equipment is not insignificant. In addition, equipment engineers are reluctant to modify existing equipment designs to allow the addition of sensors and associated hardware, because such changes could affect process stability and this work is expensive. Also, if the metrology portion of the equipment goes down during production, the equipment must also be taken down to allow repairs to be performed, reducing the throughput of the machine. For these reasons, the next paradigm shift might be from sensors on the *equipment* to sensors on the *wafer*.

Such on-wafer sensors could provide the same information about the wafer and process state as is currently available through equipment-based *in-situ* sensors, but without the added cost and complexity of integrating the sensor onto the equipment. Such a wireless sensor-wafer could be loaded into a boat along with product wafers and sent into the processing chamber. Then, as the sensor-wafer is processed, it would either transmit out (via RF, IR, or other wireless method) or record in on-board memory the measurement data. In this way the same process information is

gleaned, but with minimal invasion into the process chamber.

For this research project, an etch-rate / film-thickness sensor is investigated. However, many of the difficult issues with building an on-wafer *etch-rate* sensor are in fact general to the problem of building *any type* of on-wafer sensor.

In this paper, the feasibility of such an on-wafer, spatially-resolved etch-rate / film-thickness sensor is investigated. Also, the design, fabrication and testing of several sensor test designs are discussed. Finally, the application of the results obtained from this study to other on-wafer sensor types is presented.

1.1 Etch-rate Sensor Applications

Spatially resolved *in-situ* etch-rate sensor-wafers would have many important applications in the semiconductor processing industry. These include:

- ◇ Process Characterization / Design

One of the more obvious applications is spatial uniformity characterization during design and development of etch equipment. The current equipment development procedure is to process a set of dummy wafers, measure etched wafer parameters, adjust the machine parameters (chamber geometries, etc.), and then repeat the process. Because this process is typically repeated many times, and each iteration can take a number of days, the entire process can take several months. The reason that such a lengthy procedure is required is that with post-process measurement, only an integrated effect is measured. With a real-time measurement scheme, far fewer iterations could be performed because much more information is conveyed during each iteration.

- ◇ Process Calibration

A similar application for *in-situ* sensors is process parameter adjustment. Traditionally, dummy wafers are put into the production flow every so often, and measurements from these processed wafers are used to monitor and adjust the process. Typically, about 10% of the production flow is wasted on process characterization. An alternative to this procedure that is offered by *in-situ* sensors is real-time control. By placing an autonomous etch-rate sensor into the process chamber and closing a real-time control-loop around the tool, process parameters can be optimized automatically, in one step. By using this method, far fewer test wafers would be needed, thereby improving the throughput of the equipment.

- ◇ Equipment Diagnosis

Another use for *in-situ* etch-rate sensors is for equipment diagnosis. If a tool in a fabrication facility is malfunctioning, the repair staff needs a quick method of determining the source of

the problem, without lengthy disassembly procedures. Typically, the diagnosis of an equipment problem takes several hours. Sometimes, this involves venting and disassembling the process chamber to place wired sensors on the wafer-chuck. By instead using an *in-situ* sensor, possible sources of the problem can be eliminated or confirmed more rapidly than by using this disassembly procedure. In a typical fabrication facility, machine downtime accounts for 10% of the total equipment time. By reducing this downtime, substantial improvements in throughput can be realized.

◇ General Microsensor Technology

A very important extension for etch-rate sensors is for other microsensor applications. Because an etch-rate sensor must have on-board power and communications, as well as integrated environmental isolation, this technology can be applied to other microsensor products to make them autonomous. Currently, a multitude of MEMS products exist to measure and actuate; however, very few options are available for power and communications [1].

1.2 Available Etch-Rate Sensors

There are currently several available etch-rate sensing technologies, including full-wafer interferometry, optical-emission spectrum (OES) based methods, and ellipsometry.

Full-wafer interferometry is a method by which light is directed onto the wafer while it is being etched. A charge-coupled device (CCD) camera is then aimed at the wafer, and the reflected light intensity is recorded. In this way, each pixel of the CCD functions as an interferometer[2]. Because the light is incident on a thin-film layer, some of the light is reflected from the top surface of the film, and some is refracted into the layer and then reflected from the bottom surface. In this way, the two rays of light traverse different distances to arrive at the CCD, so they interfere with one another. Therefore, as the film thickness changes (due to the film being etched) the path-length difference changes, so the recorded light intensity goes through interference minima and maxima in time. Hence, at each pixel of the CCD the light intensity is sinusoidal, with an approximately linearly changing phase and an increasing magnitude due to less absorption into the thinning layer (see Figure 1.1). By analyzing the phase of the signals generated at each pixel of the CCD, the spatially-resolved film thickness can be determined to within about 100 Å, and etch endpoint can be determined correctly[3]. The cost of the equipment in such a system is relatively low (\approx \$20,000), because the light emission from the plasma can be used as the light source, so all that is necessary is a CCD camera. The real cost of the system lies in the work required to integrate the CCD onto the equipment. Because the CCD needs a direct view of the wafer, it is difficult to find a location for it without disrupting other etcher components.

The optical-emission spectrum for a plasma process is the intensity vs. wavelength informa-

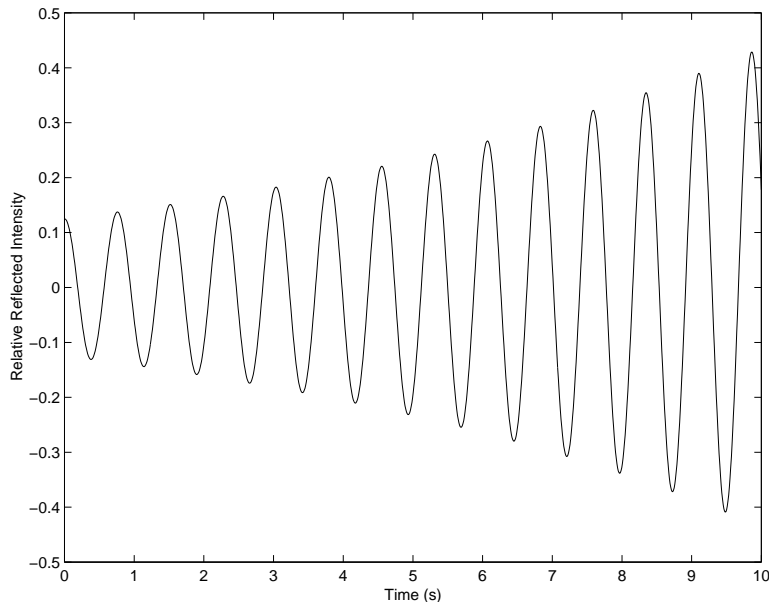


Figure 1.1: Sinusoidal interference signal.

tion for the light emitted by the plasma. This spectrum contains information about the quantity and type of gases present in the plasma, thereby conveying information about the etch process and wafer state. By aiming a spectrometer at different parts of the wafer, and by applying various reduction techniques to this emission spectrum data, etch-rate uniformity and spatially resolved endpoint can be estimated[4], as well as various other process parameters[5]. This measurement system, including spectrometer, CCD, and optics typically costs in the \$50,000 range.

Ellipsometry is a technique that yields very accurate ($\pm 4 \text{ \AA}$) measurements of film-thickness and index of refraction for a thin film. By illuminating the film with linearly polarized laser light at a glancing angle and measuring the polarization of the reflected beam, the layer thickness and index of refraction can be determined. Because the reflectivities in the perpendicular and parallel directions differ depending on the thickness and optical properties of the film, measurements of the relative intensities in each direction yields an estimate of the film thickness[6]. Due to the increased complexity of this measurement scheme, ellipsometers typically cost more than the previous two metrology schemes, around \$100,000.

1.3 Chosen Metrology Scheme

In this paper, an *in-situ* etch-rate sensor on a wafer is discussed. For such a sensor, it was decided that the following features would be necessary:

- ◇ Array of ≈ 100 film-thickness sensors on a standard-size Si wafer
- ◇ On-board power source
- ◇ On-board communications
- ◇ Environmental isolation
- ◇ Addressing scheme to enable / interrogate sensors individually

Given the above list of features, the resultant sensor will have significant monetary cost. The prototype system (see Chapter 5) is built in a full CMOS process on a 4" wafer, which is expensive (approximately \$5000 for this sensor). Building a similar sensor on a production-size wafer (8" or even 12") would cost exponentially more. In addition, a completed sensor can only be used for a very limited number of runs, because the sensors are being destructively etched during the process.

This cost is prohibitive for a real-world application. However, a technique called "flip-chip" mounting could reduce the cost of the sensor significantly. Essentially, the base (assume 8") production wafer would undergo minimal processing to create a "breadboard" of low-resolution metal lines on the wafer. Then, small diced chips from a cheaper process would be flipped over and bonded to the base wafer using flip-chip bonding. The base wafer would then serve to connect the sensors together, as well as make connections to similarly bonded power and communications modules. Using this technique, the cost could be significantly reduced. For a full-size 8" wafer with two metal layers and two intermetal dielectrics, the cost would be approximately \$300. And for a small wafer, low resolution CMOS process, the cost could be as low as \$5 / chip. Therefore, for a fully-functional production-size sensor wafer, the cost would be about \$500 (ignoring the cost of the power and communications modules, which would be the same in either case). Because a typical fabrication facility spends around this amount on a dummy wafer and the associated metrology time, this is clearly an attractive alternative both functionally and economically.

1.4 Summary of Project

For this project, three on-wafer *in-situ* etch-rate sensors were designed and fabricated. Tests were performed on each to determine operating parameters such as functionality, accuracy, and repeatability.

The first sensor design was a proof-of-concept, to see if an embedded four-point-probe technique (see Chapter 3) for measuring film-thickness was feasible. This design consists of a set of embedded four-point probes fabricated on a silicon wafer using a custom four mask process. Each probe is isolated from the others, and each has contact points for external power and data

processing. For these reasons, this design was able to test the sensor concept, but lacked the ability to perform spatial measurements or basic signal conditioning. This design was bench tested, and it was found that problems with the fabrication process rendered the design inoperable.

Because of the failure of the first design, the decision was made to go on to a more complicated second design which incorporated more features. This design was fabricated using a full 12 mask $1.3\ \mu\text{m}$ CMOS process, the **UC Berkeley Baseline CMOS process**, at the **UC Berkeley Microfabrication Laboratory**. In the second design the four-point probe sensor method is used, but four different variations are included at each sensor location, to test different sensor structures. Fifty-seven such sensor groups are spread across the surface of the wafer, and all of the sensors are interconnected. Using a novel addressing scheme, all of the sensor groups can be interrogated from a single external contact point. In addition, on-board circuitry provides basic power conditioning and data switching for the sensor. This design was bench-tested to assess functionality. It was found that while the sensors themselves functioned, the multiplexing electronics failed. Therefore, wires were directly bonded to the sensors, and an *in-situ* XeF_2 etch experiment was conducted. Several small problems made it impossible to assess the accuracy of the sensors.

A third design was fabricated which was meant to handle the problems encountered with the second design. This design was fabricated in a much more simple process, to make the time-to-experiment shorter, and features were added to make the measurement more robust and easier to make. This sensor was tested in the XeF_2 reactor during several etch cycles, and data was recorded. Polysilicon thickness measurements generated by the sensors were found to be accurate to within 1%, when compared to reference measurements made using a reflectometer.

1.5 Organization

The remainder of this thesis is organized as follows. First, a general discussion of sensor arrays is undertaken: general requirements, associated difficulties, and possible solutions are discussed. Next, three prototype etch-rate sensor designs are presented, and test results from each are reported. Finally, a summary of the ideas presented and the results obtained during this project is provided.

Chapter 2

Autonomous Sensor Arrays

In developing an autonomous sensor wafer, several issues become important. These issues can be grouped into three main categories: power, communications, and isolation.

2.1 Power

An *in-situ* etch-rate sensor wafer must contain some type of wireless, regulated power source to provide power for the electronics and sensors. There are several constraints on such a power source. As stated, it must be wireless, because one of the major goals of this project is to construct a sensor wafer that resembles as closely as possible an actual product wafer, to avoid problems with loading and unloading it from the chamber. This clearly precludes the use of wired connections to the wafer. Also, to avoid problems with wafer-handling robotics, the protrusion of the power source above the wafer surface must be limited to about 3mm. Another requirement for the power source is that it does not take up excessive area on the wafer. The smaller the power source, the more space is available for sensors. Lastly, the power source must be capable of supplying roughly 5V output, with a minimum of 1mA current, for at least 5 minutes. This is approximately the amount of power required to keep electronics and sensors running for the duration of the etch process (including loading and unloading).

Given these constraints, several power-supply opportunities exist. The primary candidate is battery-power. A range of thin, high-power batteries exist, ranging from commercial 1mm-thick watch batteries capable of 25 milli-amp hours (mAh), to research-grade 10 μ m-thick thin-film batteries capable of 100 micro-amp hours (μ Ah)[7]. In between these ranges lie a number of candidates for on-board power. While batteries are able to provide adequate power levels to the sensor, they have a few downsides. The main problem is size. Although some batteries, such as the thin-film batteries, are very thin, they have limited energy density. For this reason, they must occupy a large area of the wafer to store enough energy. If thicker batteries are used, then less area can be occupied, but the thickness becomes a concern. Another problem with using batteries as a

power source is isolation. Some of the high energy-density batteries use exotic materials such as lithium metal and V_2O_5 aerogel[8]. Isolating these materials from the etch environment becomes a critical problem.

Another possibility for a power source is the photovoltaic cell. In several processes, plasma is used. Because the plasma emits intense visible light at a range of wavelengths, this light could be used as a power source. In non-plasma processes, an external laser could be focused on the photovoltaic cell to provide power from outside the chamber. Currently available commercial photovoltaic cells are capable of 15% efficiency[9], and the broadband light power density available from plasma emission inside the chamber is roughly $1 \frac{\text{mW}}{\text{cm}^2}$ [10]. Therefore, to provide a power of $5V \times 1\text{mA} = 5\text{mW}$, a photovoltaic cell would need to have an area of:

$$\left(\frac{1}{15\%}\right) \frac{5\text{mW}}{1 \frac{\text{mW}}{\text{cm}^2}} = 33\text{cm}^2 \quad (2.1)$$

This area is clearly too large for this application, because it would cover too much of the wafer. However, by using a laser light source with a $30 \frac{\text{mW}}{\text{cm}^2}$ (typical of a “pen laser”), this area could be reduced to 1.1cm^2 . This is a very acceptable size for the power source. One limitation of this method is that several process chambers don’t have a line-of-sight view of the wafer from outside the chamber, while other processes, such as lithography, would be detrimentally affected by external irradiation.

Other, more exotic power sources exist, such as using a large capacitor to store energy for the sensor. In such a scenario, the capacitor would be charged up by an external power source prior to being placed into the processing equipment. Then, while the sensor is being processed, the capacitor would be discharged to provide power for the sensor. The main problem with this idea is that, for the typical power levels needed by the sensor, the capacitor would have to be very large. For example, assuming the capacitor starts out charged to 10V, and assuming the dielectric is SiO_2 , then the minimum capacitor thickness is dictated by the breakdown voltage of SiO_2 ($\approx 10^7 \frac{\text{V}}{\text{cm}}$):

$$x_{ox,min} = \frac{10V}{10^7 \text{cm}} = 5\text{nm} \quad (2.2)$$

Assuming a constant discharge current of 1mA, a minimum voltage requirement of 3.5V, and a required on-time of 5 minutes, the required capacitor area is given by:

$$\frac{dV}{dt} = \frac{-Ix_{ox}}{\kappa_{ox}\epsilon_0 A} \Rightarrow A = \frac{Ix_{ox}t_{final}}{\kappa_{ox}\epsilon_0 (V_0 - V)} = 6.7\text{m}^2 \quad (2.3)$$

This is clearly a much larger area than is available on a wafer. Even if novel high-density structures are used to improve the capacitance to area ratio, very large areas would still be required. For this reason, capacitive power is not reasonably feasible.

Given the available power sources, the battery was chosen as the most compatible with the design goals. Because it is able to supply the required power while occupying a small enough

volume, it is the most feasible of the power supply choices. Also, the battery power source is the most equipment-independent choice. Because it doesn't require a line-of-sight view to the outside (like the photovoltaic power source does), and it doesn't depend on the process itself for power, it can be used in many different types of equipment with minimal modification.

2.2 Communication

For an *in-situ* sensor wafer to be useful, the data it measures must be communicated to the outside world. Therefore, several restrictions exist for the sensor's communications system. First, the system must be capable of handling measurements from about 100 sensors, each operating at a minimum frequency of 1 Hz. Second, the communications system must allow a full-scale film-thickness measurement of at least $0.5\ \mu\text{m}$ with a precision of at least 1 nm. This means that it must have at least 9 bits of precision ($\frac{500\text{nm}}{1\text{nm}} = 500 \approx 2^9$). Therefore, the overall communications bandwidth must be at least $(100\text{ sensors}) * (1\text{ Hz}) * (9\text{ bits}) = 900\text{ Hz}$. Another requirement for the communications system is that it uses very little power. Because the power source is only capable of delivering a limited amount of power, the communications system must use only a fraction of this amount. For the same reasons as for the power supply, the communications system must be wireless, and must fit within the same size constraints. Lastly, the communication system must not, as much as possible, depend on the particular geometry of the etch-chamber. For example, if optical communications is used, the light-source must not be directed only toward the view port in a particular type of etcher, because then this sensor would be useless in other etch equipment in which the viewport is situated differently with respect to the wafer chuck.

For a multi-sensor wafer the communications can be either modular or central. For modular communication, each sensor (or possibly each group of sensors) would have its own communication system, so that the sensors transmit their data in parallel. With central communications, all of the sensors are connected to a central communications system, which communicates the data for the entire wafer. Different communications methodologies usually lend themselves more to one of these techniques than the other.

Perhaps the easiest communications option is optical transmission. With this method, a light emitting diode (LED) on the wafer transmits the sensor data to a photo-sensitive receiver outside the chamber using some type of frequency-modulation scheme. This method has the disadvantage that a line-of-sight path to the wafer is required. In many cases, such a view port exists, but in several types of processing equipment this is not possible. This technique can be used with either modular or central communications, but because LED power requirements are relatively high, and modular communications would require many LEDs on the wafer, this method is less advantageous. Therefore, for an optical scheme, centralized communications would most-likely be employed.

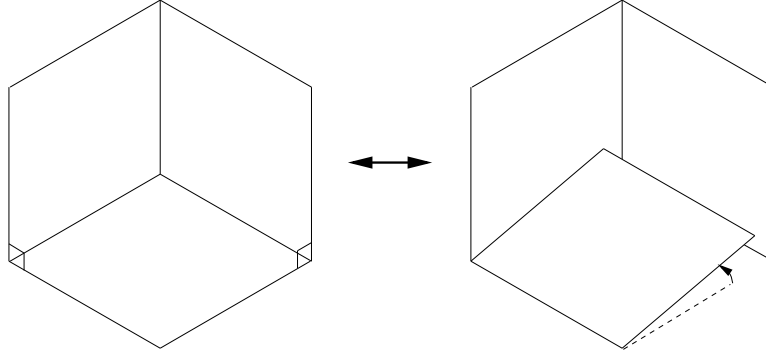


Figure 2.1: MEMS corner-cube retroreflector

Using radio-frequency (RF) communication is also an option. By placing an RF oscillator and modulation circuitry on the wafer, etch-rate data can be transmitted out of the chamber to external receiver circuitry. This has the advantage that it does not depend on chamber geometry (placement of viewports, etc.) as much as optical transmission. In addition, for plasma etch processes, the plasma itself forms a conductive cloud around the wafer, impeding RF transmission. Another downside to using RF is the complexity of RF transmission circuits and their high power requirements. Because of these requirements, centralized communications techniques would be used for RF.

A third possible communication system is the so-called corner-cube retroreflector. This microelectromechanical system (MEMS) consists of a microfabricated corner-cube reflector (three mutually orthogonal reflective planes placed together as shown in Figure 2.1) with a hinged bottom reflector. When the bottom plane is in the orthogonal position (left side of Figure 2.1), light rays that strike the corner cube are reflected off all three planes, and travel exactly back to their source. However, when the bottom plane is actuated out of the orthogonal position (right side of Figure 2.1), incoming light rays do not return to their source. Therefore, information can be modulated onto an incoming beam of light and reflected back to its source. The major advantage of this method of communication is that it requires very little power. Since the only power required is that needed to electrostatically move the bottom plate, which typically weighs about $2 \times 10^{-10} kg$, *extremely* low power levels are needed. Also, bit-rates of up to $10 kHz$ have been achieved using these devices[11], which is more than that required for the etch-rate sensor. Because they require such low power, and can be interrogated by a directed laser beam, modular communications techniques would probably be used. One retroreflector could be placed next to each sensor, and the scanning laser would read the etch-rate for the sensor nearest the laser spot. A number of disadvantages exist, however. First, because these MEMS retroreflectors are typically constructed with polysilicon beams and gold reflecting surfaces, they are not well adapted to withstand etch processes. Also, the gold surfaces are likely to contaminate the etch chamber with gold, a severe problem for CMOS devices.

Another problem with this method is that it requires a directed line-of-sight view of the wafer so that a laser can be focused on the retroreflector. As with optical communications, this makes the design very equipment-dependent. One last problem with typical MEMS retroreflectors is that because they are electrostatically actuated, very high voltages (≈ 100 V) are required. While the *power* supplied is still within available power-supply limits, this high voltage poses problems.

Given the available communication system choices, the most feasible choice seems to be optical communication. The power requirements for this method are well within the capabilities of the power supply, and the equipment dependence is minimal. The only requirement is that there be a viewport with a line-of-sight view of the wafer. Because the transmitting LED can be omnidirectional, it does not need to be pointed in a particular direction, so any viewing direction will work. LED communication is also very capable of handling the necessary bandwidth. Finally, the transmitting LED can be easily isolated from the environment by coating it with a thin layer of SiO_2 which is transparent to many wavelengths of light.

2.3 Isolation

Because most of the processing techniques used in the semiconductor manufacturing industry place the wafers in “harsh” environments, any sensor that will be processed by the equipment needs to have some type of isolation from the environment. The main conditions that would be detrimental to a sensor wafer are high temperature and electrical noise. Also of importance are chemical attack and physical damage (such as etch damage).

In rapid thermal processing (RTP), for example, the temperature typically exceeds 1000°C . Any electronics on the wafer that are not isolated will stop functioning above about 150°C , and will physically melt above 660°C (the aluminum interconnect melting temperature). Therefore, any sensor that might operate in this environment *must* be thermally shielded so that the electronics remain at a lower temperature.

In plasma-etch environments, the plasma is created by coupling radio-frequency (RF) power into a gas. Because of this high-power RF energy, surface currents are generated in exposed, unshielded conductors on the wafer surface. Therefore, if electronics are functioning on the wafer (as in the case of a sensor-wafer), then these generated currents might interfere. So a sensor wafer taking measurements inside a plasma chamber must be electrically isolated from the plasma environment to function properly.

One possible option to isolate the electronics and sensors from electrical noise is to add a metal layer over all of the electronics (but isolated by an oxide), and have a contact from this overcoat to the substrate. In this way, the top metal layer would shield the electronics below by providing a ground path. One downside of this method is that the extra layers add complexity to the structure of the sensor wafer, adding to the cost. Also, this type of isolation could not be used

over the etch-rate sensor, because it would obstruct the operation of the sensor.

The main method for offering shielding from chemical and physical attack are through the use of some type of overcoat. By covering the electronics, and possibly the sensors, with an oxide layer, for example, most chemical and physical processes would only attack the oxide and not the underlying electronics. When used in conjunction with the metal layer described above, this method provides isolation from electronic, chemical, and physical problems. The downsides are, as with the metal layer, added process complexity and inability to cover the etch-rate sensors.

To isolate electronics from high temperatures, more complex measures need to be taken. One method for providing this isolation is to create a microfabricated “vacuum chamber” around the electronics, so that thermal conduction and convection are virtually eliminated[12]. Then, by adding appropriate coatings to the walls of the chamber, radiation heat transfer can be minimized. The process to achieve an evacuated chamber around electronics is somewhat complex, but Klaassen[13] has successfully fabricated thermally isolated RMS power sensors for RF applications.

The basic process flow is as follows: first, electronics are fabricated in the n-well of a standard CMOS process. Then, using a MEMS post-process technique, a selective wet etchant, TMAH, is used to etch away the surrounding silicon, while leaving the n-well where the electronics are untouched[12]. Once the etch has proceeded to completion, the electronics are left “floating” over a void. Then, by coating the electronics with an oxide layer, covering this oxide with a nitride layer, and then wet etching the oxide out from under the nitride, a “bubble” over the electronics is formed. By performing this last etch step in the correct environment, the interior of the chamber can be filled with a number of gases, or left as a partial vacuum. This process therefore achieves the desired result: CMOS electronics enclosed within a vacuum chamber. Then, by applying metallic coatings to the exterior of this chamber, radiation heat transfer is reduced.

The major downside to this method of isolation is added process complexity. The process to create thermally isolated electronics is very complicated, adding several masking and processing steps in addition to the standard CMOS process used to fabricate the electronics. This added complexity adds significant cost to the sensor. The main benefit of this process is simply that it offers excellent thermal isolation. Techniques such as this are the only ones that offer a low enough thermal conduction coefficient, so that temperatures of 1000°C can be withstood for several minutes while maintaining an interior temperature below 100°C . These are the typical RTP processing conditions; therefore some type of thermal isolation such as this is necessary if sensors are to be put into an RTP process.

For the etch-rate sensor, the thermal isolation is not necessary, as the wafer remains below 100°C in most plasma chambers. However, some type of electrical, physical, and chemical isolation techniques must be used to isolate the wafer from the plasma environment. The most reasonable choice to accommodate all three requirements is to coat the electronics with an oxide-conductor-oxide sandwich. The oxide layers protect the electronics from physical and chemical

attach (assuming the etch chemistry is not designed for oxide), and the conductor layer forms an isolation ground plane.

Chapter 3

Etch-Rate Sensor Methodology

To measure etch-rate of a thin film, one must measure film-thickness as a function of time. A number of measurement techniques exist for measuring film-thickness, several of which are applicable to an on-wafer sensor.

3.1 Mechanical Techniques

A vibrating structure, such as a cantilever beam, has a specific natural frequency. In such a structure, if the beam is excited into vibration by an external energy source and then left free, it will vibrate at precisely this natural frequency. For a cantilever beam, the natural frequency depends on the geometry of the beam (which helps determine the spring constant), the mass of the beam, and the damping present in the beam. Therefore, for a beam in which the mass is changing, but the spring constant and damping constant remain fixed, this natural frequency changes. So a free-standing beam whose end-mass is being etched away can serve as a film-thickness measurement device. Small beams of this type are commonly constructed out of quartz crystals, with piezoelectric transduction of the crystal motion, for use in evaporative deposition systems. In this application, the material being deposited is also deposited on a sacrificial quartz beam, so that the increased beam mass changes the natural oscillating frequency. The beam is driven by piezoelectric actuators, and its position is also sensed with piezoelectric force sensors. Simple electronics deliver an unstable driving force to the beam to cause it to oscillate. Such sensors can be extremely sensitive, because they are interrogated by measuring a frequency, which can be measured with *very* high precision ($\pm 0.00001\%$). The downside of using such a technique in an on-wafer sensor is that the oscillator structure and associated drive and sensing elements must be fabricated onto the wafer. Because the oscillator sticks up off the wafer surface and is vibrating, etch-rate will most likely be altered near the sensor.

3.2 Optical Techniques

Another technique for measuring film-thickness is by using a reflectometer. This involves illuminating the surface of the wafer with a light source and measuring the reflected intensity at either a single wavelength or at many wavelengths. If a single wavelength is used, the intensity versus time curve is used to determine the layer thickness. Because the layer under observation is being etched away, its thickness is decreasing. Since the interference minima and maxima depend on the thickness of the reflecting layer, the intensity of the reflected light varies with layer thickness. Therefore, by observing the rate at which the reflected intensity is changing, the etch rate can be calculated. Given a known starting thickness, the overall layer thickness can be extracted by integrating the etch-rate over time. For a multiple wavelength reflectometry system, the layer thickness can be inferred at each time point. Based on the intensity versus wavelength data, the thickness of the layer can be determined based on the wavelength difference between interference maxima and minima. Both of these techniques are capable of measuring film-thicknesses with a high degree of accuracy (roughly 20 Å precision), over a wide range of thickness values (typically between 20 Å and 15μm). However, such a system would be basically impossible to implement for an on-wafer sensor since it requires equipment (the light source and light sensor) external to the wafer being measured.

3.3 Electrical Techniques

Another sensor that can be used to make film-thickness measurements is the four-point probe. This device is most commonly used to measure the sheet resistance of a thin film layer. For a chunk of material of uniform material properties, if four electrical probes are contacted to the surface in a linear arrangement, and a current flows into and out of the outer two probes, then the voltage measured across the inner two probes can be shown to be [14] (see Appendix A.1 for more detailed derivation of four-point probe physics):

$$V = \frac{\rho I}{2\pi F} \left(\frac{1}{s_1} + \frac{1}{s_3} - \frac{1}{s_2 + s_3} - \frac{1}{s_1 + s_2} \right) \quad (3.1)$$

where ρ is the resistivity of the layer, I is the current passed through the outer two probes, F is a non-dimensional geometrical correction constant, and s_1, s_2 , and s_3 are the three distances between the four probes. The F in Equation 3.1 corrects the equation for deviations from the ideal geometry, which is a slab with an infinite planar surface, and infinite depth. If the sample is instead a very thin sheet (thickness t) of material with large area (see Figure 3.1), and if the probe spacing is uniform ($s_1 = s_2 = s_3 = s$), then $F = \frac{t}{2s \ln(2)}$, and Equation 3.1 can be rearranged to find the thickness, t :

$$t = \frac{\ln(2)\rho}{\pi} \frac{I}{V} \quad (3.2)$$

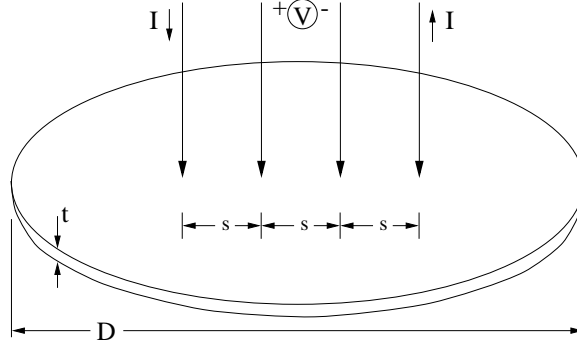


Figure 3.1: Collinear four-point probe arrangement. Note $D \gg s$.

This equation relates the layer thickness to the measured voltage, the sourced current, and the resistivity of the material. Therefore, this device can be used as a thickness measurement device. Because the measurement is a purely electrical measurement, no moving parts are involved, and the measured material can have a planar shape. For these reasons, a thickness measurement based on the four-point probe is minimally invasive and very accurate.

3.4 Project Decision

Based on the characteristics of the film-thickness sensors discussed above, the four-point probe was chosen for this project. Because of its ability to measure film-thickness in a minimally invasive way (electrical measurement of a non-moving flat structure), the four-point probe promises to be the most accurate sensor. Also, the structure of the four-point probe most closely resembles an actual etched surface, so microloading and macroloading effects can be minimized.

Chapter 4

Design I – Basic Four-Point Probe

4.1 Design Concept / Details

The decision was made to design and fabricate a proof-of-concept film-thickness sensor-wafer utilizing the four-point-probe sensing methodology, with only very basic capabilities. The goal of this design was to demonstrate that the chosen sensor structure was indeed able to measure etch-rate in real time.

4.1.1 First Test Design

The first etch-rate sensor design iteration consisted of a simple four-point probe measurement device fabricated on a silicon wafer. Each sensor takes up about 0.64cm^2 , and 88 separate sensors fit on a single 4" silicon wafer. For simplicity, each sensor on the wafer functions independently, and metal contacts pads are attached to each of the sensors for connecting to external current sourcing and voltage measurement equipment. In this way, wires can be bonded to the contact pads and the wafer can be inserted into the etcher for testing (see Section 4.2).

A simple process was chosen to construct this simple sensor design, and all fabrication work was performed in the **UC Berkeley Microfabrication Facility**. The layout was designed using **AutoCAD R12**. The measured layer is the top polysilicon layer in the process. The four-point probe region has the cross-sectional structure shown in Figure 4.1, and the simplified fabrication

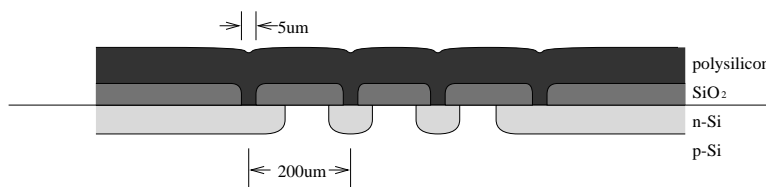


Figure 4.1: Cross-section of four-point probe region.

- ◇ Pattern with WIRE
- ◇ N+ S/D Implant: Arsenic 160 keV $5E15/cm^2$
- ◇ Wet oxidation at $1000^\circ C$
- ◇ Pattern with CONTACT / etch oxide
- ◇ Deposit poly (4500 Å)
- ◇ Pattern with PAD / etch poly
- ◇ Sputter $0.6\mu m$ Aluminum
- ◇ Pattern with ALUM / etch Aluminum

Figure 4.2: Simplified fabrication process for four-point probe sensor wafer.

process is given in Figure 4.2.

Essentially, buried interconnections (diffused n-type regions in the p-type substrate, isolated from one-another by reverse biasing the substrate/contact junction) are used to make electrical contact from four aluminum contact pads to four points on the polysilicon layer. These four points form the four-point probe. The middle SiO_2 layer isolates the interconnections from the polysilicon layer.

The overall layout of the device is shown in Figure 4.3. The five large squares toward the top of the layout are the aluminum contact pads, for making external connections. The fifth pad, in the middle, is for external contact to the silicon substrate so that the buried interconnect junctions can be reverse-biased. The thin wire-like structures running from the contact pads toward the bottom of the layout are the buried interconnections. And the small dots at the ends of the interconnections are the contacts from the interconnections, through the isolation SiO_2 layer, to the polysilicon layer above. These are the “probes” of the four-point probe.

4.2 Test Results

4.2.1 Bench Test

Once the first sensor design was complete and the wafers had been fabricated, a bench test was performed to make sure that the static sheet resistance of the polysilicon could be accurately measured. For this test, a probe station was used to physically probe the wafer, and an external adjustable current source and digital voltmeter were hooked to the probes. The current I (see Figure 3.1) was varied between $0.0mA$ and $160mA$, and the voltage V was measured at each point. According to Equation 3.2, each of these measurement points should give the same measured sheet resistance value. However, as shown in Figure 4.4, the measured sheet resistance changes with applied current, I . In addition, at all of the current/voltage points the measured value of sheet resistance is far below the actual value, $27\Omega/sq$. In short, the design did not function correctly.

There are a number of factors that might explain this result. Probably the most compelling factor is leakage current. Because the “wires” that connect the probe points to the contact pads

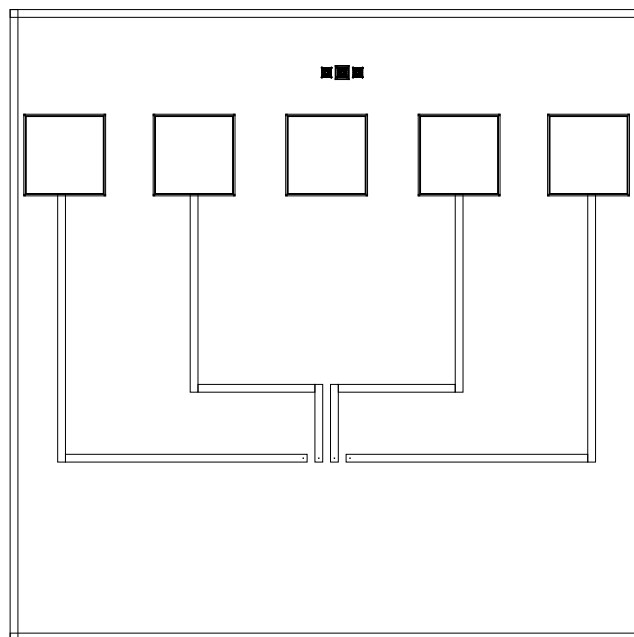


Figure 4.3: Layout of four-point probe sensor design.

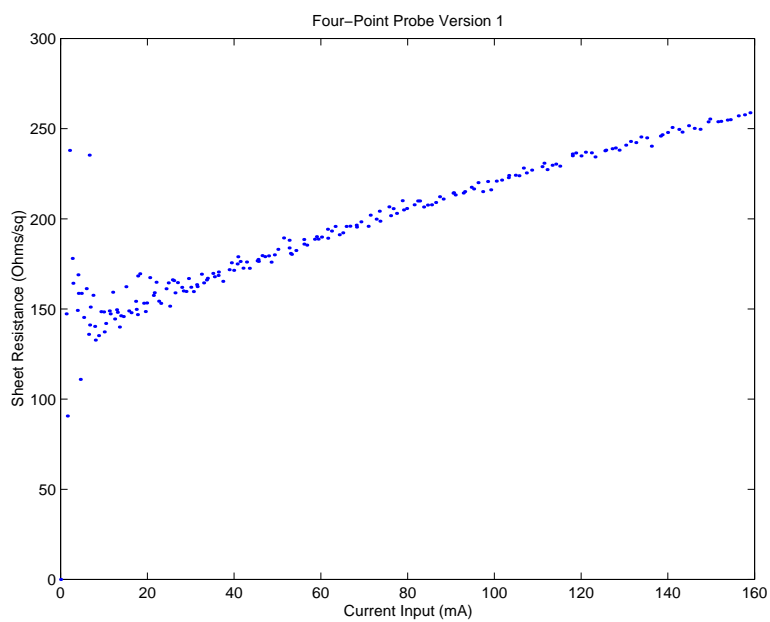


Figure 4.4: Plot of measured film sheet resistance vs. applied current

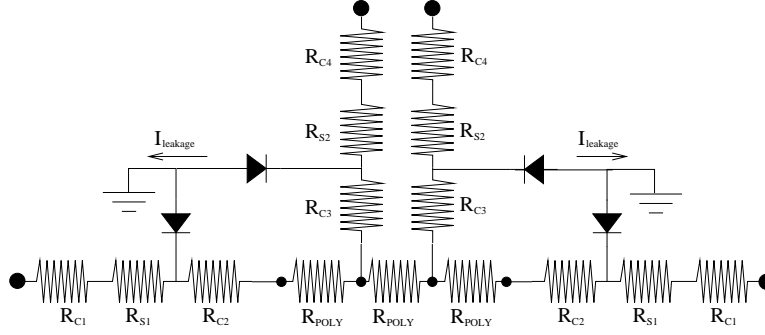


Figure 4.5: Equivalent circuit for design 1, with diffused carrier wires modeled as diodes

(Figure 4.3) are in fact diffused n-type regions inside a p-type wafer, a small leakage current is able to flow out of the wires into the substrate. Observing the equivalent circuit diagram, with the diffused carrier wires modeled as diodes (Figure 4.5), one can see that leakage currents into the voltage measurement leg of the circuit could cause gross measurement errors. In this figure, the four dark dots in the center represent the probe points, the R_{POLY} resistors are the resistance of the polysilicon layer, the R_{CX} resistors represent the contact resistances between various layers, and the R_{SX} resistors represent the resistances due to the finite conductance of the diffused-carrier wires. As can be seen from the diagram, currents flowing in the voltage measurement legs could cause voltage drops that would affect the measured sheet resistance value. In addition, because leakage current is a nonlinear phenomenon, the effects of the current could cause the nonlinear behavior shown in Figure 4.4.

Another possible reason for the design's failure is that the oxide layer between the silicon surface and the polysilicon measurement layer is very thin (100 Å), due to a processing error. Therefore, when voltages are placed on the polysilicon layer, the substrate area below the layer can become inverted, in effect connecting the probes together. This would have the same effect as the leakage current problem discussed above, and could contribute to the problems encountered with the design.

4.2.2 XeF₂ Test

After the bench test was performed, a real-time etch test was to be performed. To implement such a test, wires would need to be bonded to the contact pads on the sensor-wafer, so that they could be threaded through the XeF₂ viewport. A standard piece of semiconductor-processing equipment is the ultrasonic wire bonder, which is used to bond fine aluminum or gold wire between the contact pads on an integrated circuit to the connector pins of a chip package (see Figure 4.6). However, this equipment cannot be used to bond long ($\approx 1\text{m}$), thick ($\approx 22\text{AWG}$) wires to a wafer for the purpose of passing them into the process chamber, because the wire used by these machines is no thicker than about 0.125 mm (36 AWG). Therefore, a novel method of bonding long wires to

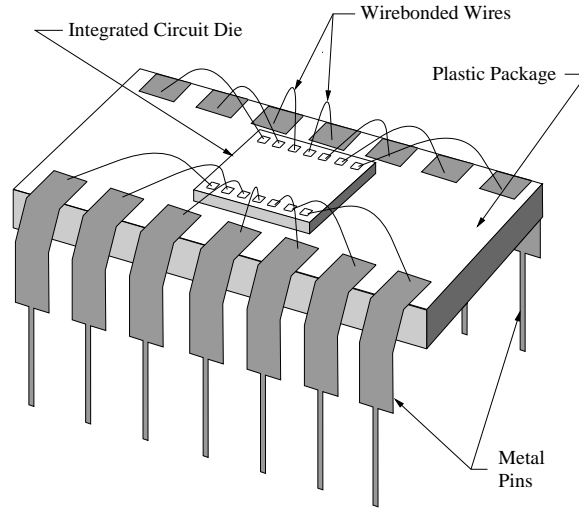


Figure 4.6: Integrated circuit die wirebonded to metal pins on plastic package.

a wafer was devised. Using this method, a small “strip header” was glued to the wafer near the desired wire bonding point using a vacuum-safe epoxy (tradenamed Hysol 1C). A strip header is a small strip of short (0.5cm) metal pins connected together by a piece of plastic (see Figure 4.7). Then, once the epoxy dried, one end of each metal post on the strip header was soldered to one wire of a twisted-pair bus of regular insulated wires. The other end of each metal post was then connected to the wafer contact pads using the standard ultrasonic bonding machine. In this way, electrical connections were made from the wafer to a long bus of wires (see Figure 4.8), as desired.

Unfortunately, because the sensor wafer failed the bench test, the XeF_2 etch test was never performed. However, these wire-bonding methods are useful, and they are utilized in the testing of the other sensor wafers (discussed in Chapters 5 and 6).

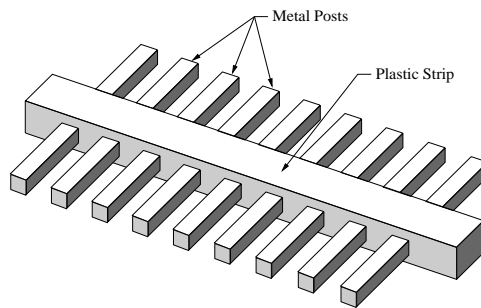


Figure 4.7: Strip header.

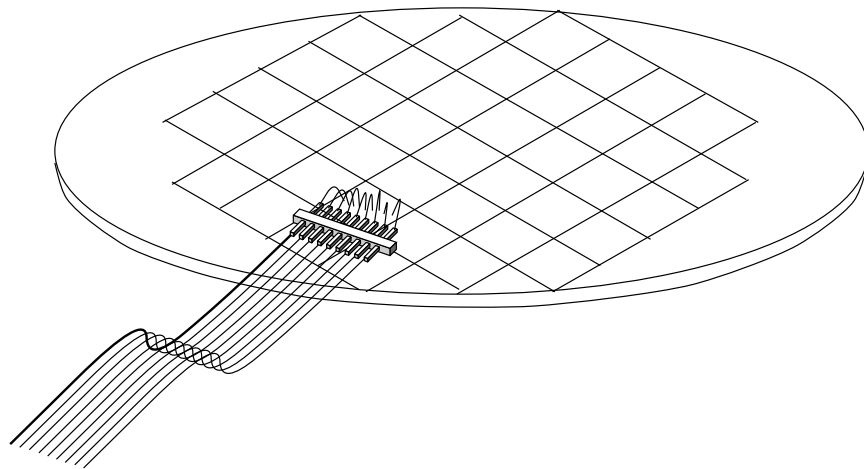


Figure 4.8: Sensor wafer with wires soldered to strip header, and strip header wirebonded to wafer.

Chapter 5

Design II – Fully Integrated Wafer

5.1 Design Concept / Details

After the first etch-rate sensor design was determined to have problems, the decision was made to begin work on a second design. Instead of attempting to redesign the first sensor wafer, it was decided that the second sensor wafer should feature more electronics integration, as well as interconnected sensors. For this design, the same film thickness measurement technique (the four-point probe technique, see Section 3.4) is used, with a few small modifications which are discussed below. However, all of the sensors on the wafer are interconnected, with an addressing and data bus scheme which allows interrogation of each individual sensor from a single point on the wafer. Further, the current source is on-board, so that a single, variable 5V supply can be used. This design was laid out using **Cadence Design Systems 97A**, and fabricated in the **UC Berkeley Microfabrication Facility** using the Berkeley CMOS Baseline process (see Appendix A.2 for a full process listing). This process is a 12 mask, double-poly, twin-well 1.3 μm CMOS process.

5.1.1 Sensor Structure

For the same reasons discussed in Section 3.4, the sensor used in design #2 is also based on the four-point probe thickness measurement technique. However, the probe geometry is no longer linear. Instead, a so-called van der Pauw structure is utilized. In this configuration (see Figure 5.1), the four probes are placed around the perimeter of an arbitrarily shaped planar region. For this structure, the measured resistivity is given by[14]:

$$\rho = \frac{\pi t}{\ln(2)} \frac{(\frac{V_{CD}}{I_{AB}} + \frac{V_{DA}}{I_{BC}})}{2} F \quad (5.1)$$

where V_{CD} is the voltage drop from probe C to probe D , and I_{AB} is the current flowing into the region from probe A and out of the region from probe B , etc. F is a dimensionless factor which

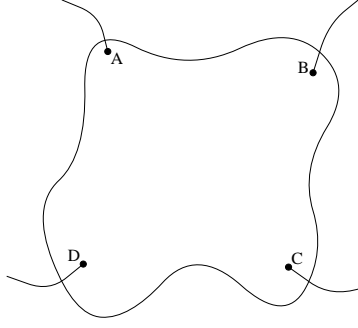


Figure 5.1: Arbitrarily shaped planar region, with van der Pauw probes attached.

depends on the shape of the planar region. For a symmetrical region (such as a square) with equidistant probing points, $F = 1$, and Equation 5.1 can be solved for the thickness t :

$$t = \frac{\ln(2)\rho}{\pi} \frac{I_{AB}}{V_{CD}} \quad (5.2)$$

This structure allows the same measurement sensitivity in a much smaller area because the probes are arranged in a square instead of a line. Another fact that allows a sensor based on this structure to be much smaller is that the probes are placed at the *edges* of the square. In contrast, with the linear four-point probe the overall dimension of the measured layer must be *much larger* than the size of the probed region (see Figure 3.1).

For design #2, a van der Pauw structure is fabricated on the gate polysilicon layer of the CMOS process (see Figure 5.2). Metal interconnections are used to connect the corners (the probed points) to the measurement circuitry. The remaining SiO_2 layers are placed over this polysilicon structure, including the overglass layer. Then, once the CMOS process is finished, a 13th masking step followed by a wet SiO_2 etch is used to selectively etch back to the polysilicon sensor surface (see Figure 5.3).

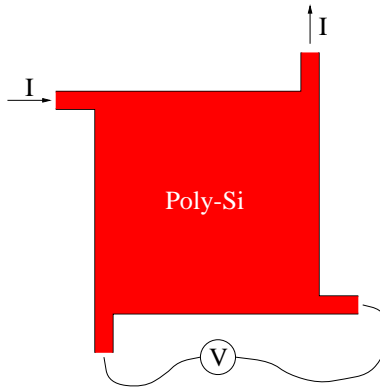


Figure 5.2: CMOS Implementation of van der Pauw probe structure on gate polysilicon layer.

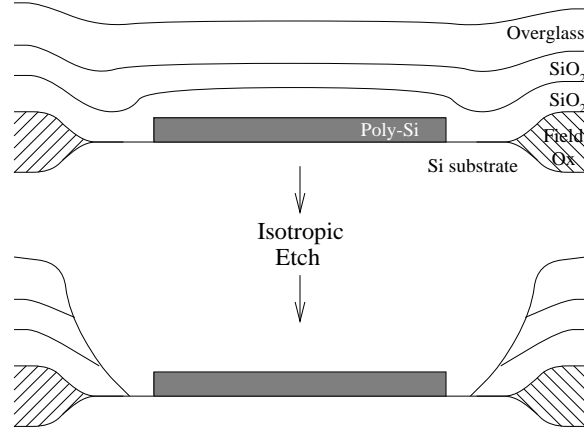


Figure 5.3: Post-process wet SiO_2 etch to expose van der Pauw plate.

The reason that the SiO_2 layers are added over the polysilicon layer is that not doing so violates an important design rule. In a CMOS process, the contact hole etch and the metal line definition etch are designed to stop on metal and oxide, respectively. Therefore, if a metal layer lying on top of a polysilicon layer is etched away, the etch will most likely etch into the polysilicon somewhat. Therefore, by cutting contact holes and etching away all metal above a polysilicon layer, there is no way to tell how much of the polysilicon will be etched away. So, to keep a smooth polysilicon surface of known thickness, it is first covered by oxide and then later exposed by a very selective wet SiO_2 etch.

Four slightly different van der Pauw structures are included in Design #2. These four sensors are individually selectable externally, and they are used to evaluate the effects of various geometrical parameters for the van der Pauw structure. Two of the structures are designed to be exposed using the SiO_2 wet etchback procedure described above, and the other two are designed with aluminum layers on top of the sensor so that aluminum wet etchant can be used. One of each of the sets of sensors is a square-shaped van der Pauw structure, and the other is rectangularly shaped. The two geometrical (square and rectangular) designs are shown in Figure 5.4.

5.1.2 Single-Die Design

In the UC Berkeley Baseline process, a **GCA** wafer stepper is used to repeatedly expose a single mask (a die) in a grid pattern across the wafer. Therefore, to interconnect all of the sensors, a technique called *field-stitching* is employed. Field-stitching simply means that the grid of dice on the wafer very slightly overlap ($\approx 5\mu\text{m}$) one-another. In this way, lines that touch the edge of one die can contact lines that touch the adjoining edge of the next die (see Figure 5.5). Therefore, by laying out wires that go from one side of a die to the other, a “bus” is created which interconnects each row of the wafer. Similarly, if wires go from the top of the die to the bottom, a column-bus is created. This is the basis for data transmission on the etch-rate sensor wafer.

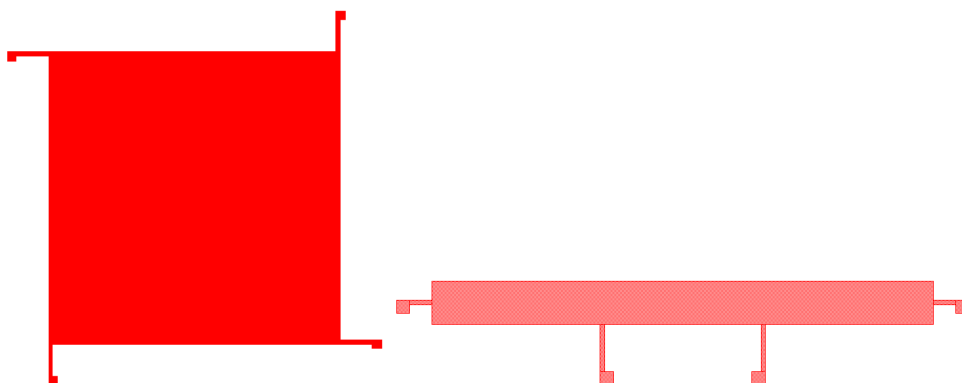


Figure 5.4: Two van der Pauw structures used in design.

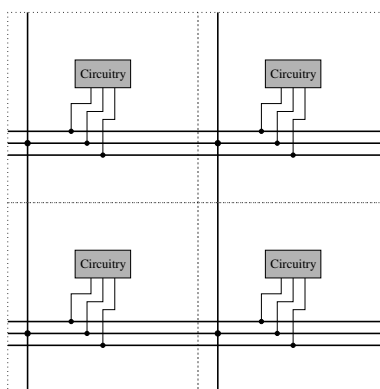


Figure 5.5: Field stitching allows wires to connect individually printed dice together.

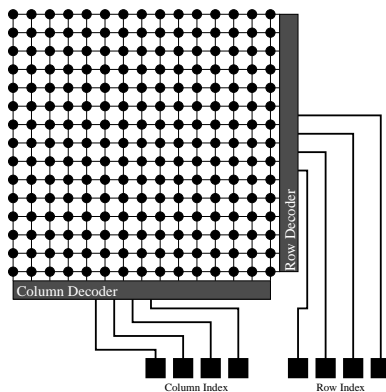


Figure 5.6: Typical row/column addressing scheme for a RAM circuit.

The ability to individually address a *particular* die on the wafer, however, is a more difficult problem. In a typical random-access memory (RAM) circuit, there is a similar need to address one particular element of a rectangular grid of memory elements (see Figure 5.6). In this case, the solution commonly used is to connect each row and each column of elements together, and activate only one row and one column at a time. Then, the element whose row and column are *both* activated turns on. This necessitates *separate* electronics (the row and column decoders) at the ends of the rows and columns to activate the proper element. In this sensor, however, there can be no row and column decoders because every die must be the same.

Another addressing scheme which one might think of would be to create a bus of wires (spanning the wafer) to carry the digital representation of the desired row number, and another bus for the column number. Then, from one die location the bus is externally probed, and the row and column number are set so that the proper die turns on. Then each die would have a comparator circuit which checks the desired address on the bus and compares it to its location to see whether or not to turn on. However, to compare the desired address with each die's location, each die would need to have a different comparator circuit so that only one die turns on at a time. Since every die on the wafer must be the same, this is not possible.

For these reasons, a more intelligent addressing scheme was developed. The scheme is based on *cyclic coding*[15]. Basically, each die contains a set of bus wires as in the previous example, but each wire is “shifted” by one position in going from one side of the die to the other, as shown in Figure 5.7. In this way, if the binary number 0010 is put on the horizontal bus of the die on the right, this pattern will be bit-shifted for the other dice in the row, so that the number 1000 exists on the bus for the die on the left. Then, if the top wire of the bus is used to activate the dice, the left die — and *only* the left die — is activated. Using the same type of bus in the vertical direction, the desired addressing ability is accomplished. (Note: For clarity, two items are left out of Figure 5.7. One is a set of wires that travel vertically to interconnect the column bus with its neighbors above and below, and a similar set to interconnect the row buses. These are necessary because the wafer

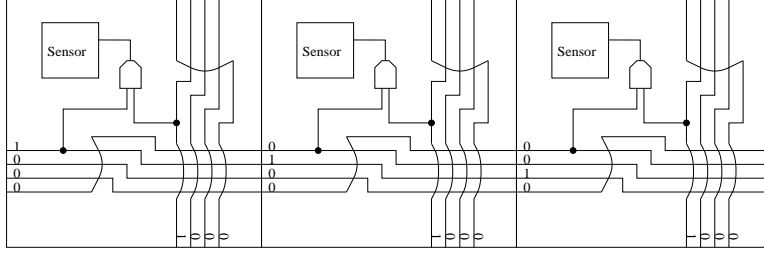


Figure 5.7: Addressing scheme based on cyclic coding.

is only probed at a single location, and without these interconnections only those buses in the row and column of the probes point would be activated. The other is a data bus which interconnects every die on the wafer, so that the sensor output data reaches all points of the wafer.)

5.1.3 Yield Enhancement Features

For a regular process run, *yield* is defined as the number of working circuits that finish a run divided by the total number that started the run. Because this field-stitching technique interconnects all of the dice on the wafer, effectively creating *one large circuit*, yield considerations become critical. One flaw anywhere on the wafer can cause it to stop working. For example, if the row-indexing bus becomes corrupted anywhere on the wafer, then the entire wafer might not function. For this reason, several design features were added to enhance yield.

A primary yield concern is a fault in the power or data bus. If a short occurs anywhere on these buses, the entire wafer will be without power or data. To keep this possibility low, the power and data bus wires were made very large ($50\mu m$ lines with $50\mu m$ space) to avoid both resolution problems and particulate contamination problems. To avoid similar problems with the row and column index buses, the wires were made somewhat large ($16\mu m$ lines with $16\mu m$ space) and a redundant set of buses was added. Therefore, if it is discovered that any of the wires in the primary bus are malfunctioning, the equivalent wires in the secondary bus can be used. In addition to these modifications, $4\mu m$ design rules were used for all electronics, even though the process is capable of $< 2\mu m$ resolution. This was done to reduce the chances of resolution-based problems in any of the electronics.

5.1.4 Power and Communications

For initial testing of this design in the XeF_2 etch chamber, wires were attached to carry power and data to and from the wafer. However, for further testing in plasma-etch environments, wireless power and communication are necessary to avoid the difficulties of threading wires through the wafer-handling robotics into the etch-chamber. To achieve this goal with the current design, separate power and communications modules will be built. These modules will consist of flat,

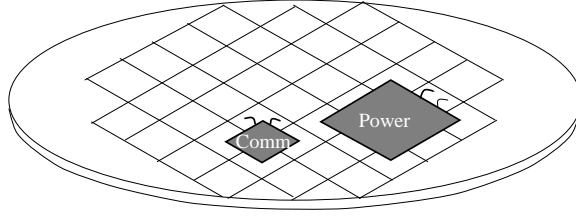


Figure 5.8: Sensor wafer with power and communications modules mounted.

thin substrates with the necessary power or communications electronics mounted on them. These modules will then be either flip-chip mounted or glued down and wire bonded to the sensor-wafer substrate (see Figure 5.8). Because such modules will be on the order of a few centimeters on a side, they will cover several of the sensors on the wafer. However, because there are 57 such sensors, this is not a significant loss. And because of the bus structure of the wafer, there are no positioning limitations on the modules. They can be placed in any convenient location (even with the power and communications modules in separate locations) on the wafer, and bonded to the nearest set of bond-pads. Also, in this way different designs for the power and communications methodology can be tested on the same substrate wafer by removing old designs and re-bonding new ones.

5.1.5 Sensor Layout

The full sensor layout is shown in Figure 5.9.

The column buses are the two groupings of horizontal wires at the bottom of the layout, and the row buses are the two vertical sets on the right. (Note that the *column* bus runs *horizontally*, and the *row* bus runs *vertically*. This might seem incorrect, but upon closer examination, one can see that the horizontal set of wires selects which die to turn on *within the row*, hence selecting the proper *column*.) The “shift” in each of the buses is located on the left side for the column buses, and at the top for the row buses. The data and power buses are the group of larger horizontal wires above the column buses, and also the group of larger vertical wires to the left of the row buses. The vertical and horizontal set of power and data wires are connected together where they cross to interconnect the entire wafer. The arrays of squares at the bottom of the layout and also toward the top-left of the layout are contact pads for external probing or wire-bonding. The set of contact pads at the bottom connects to the power and data bus, while the two sets of five contacts at the top-left connect to the row and column buses. Between the row and column contact pads and the bus wires are 5-bit decoders, which translate a 5-bit binary representation of the desired row or column into a 1-of-32 wire output, which is directly connected to the row and column buses. Between the row and column decoders, near the center of the layout, is the sensor group. Four different sensor designs are available, and one of the four is selected by two wires in the power/data bus. The current source for the van der Pauw structures is also located in this sensor group, toward

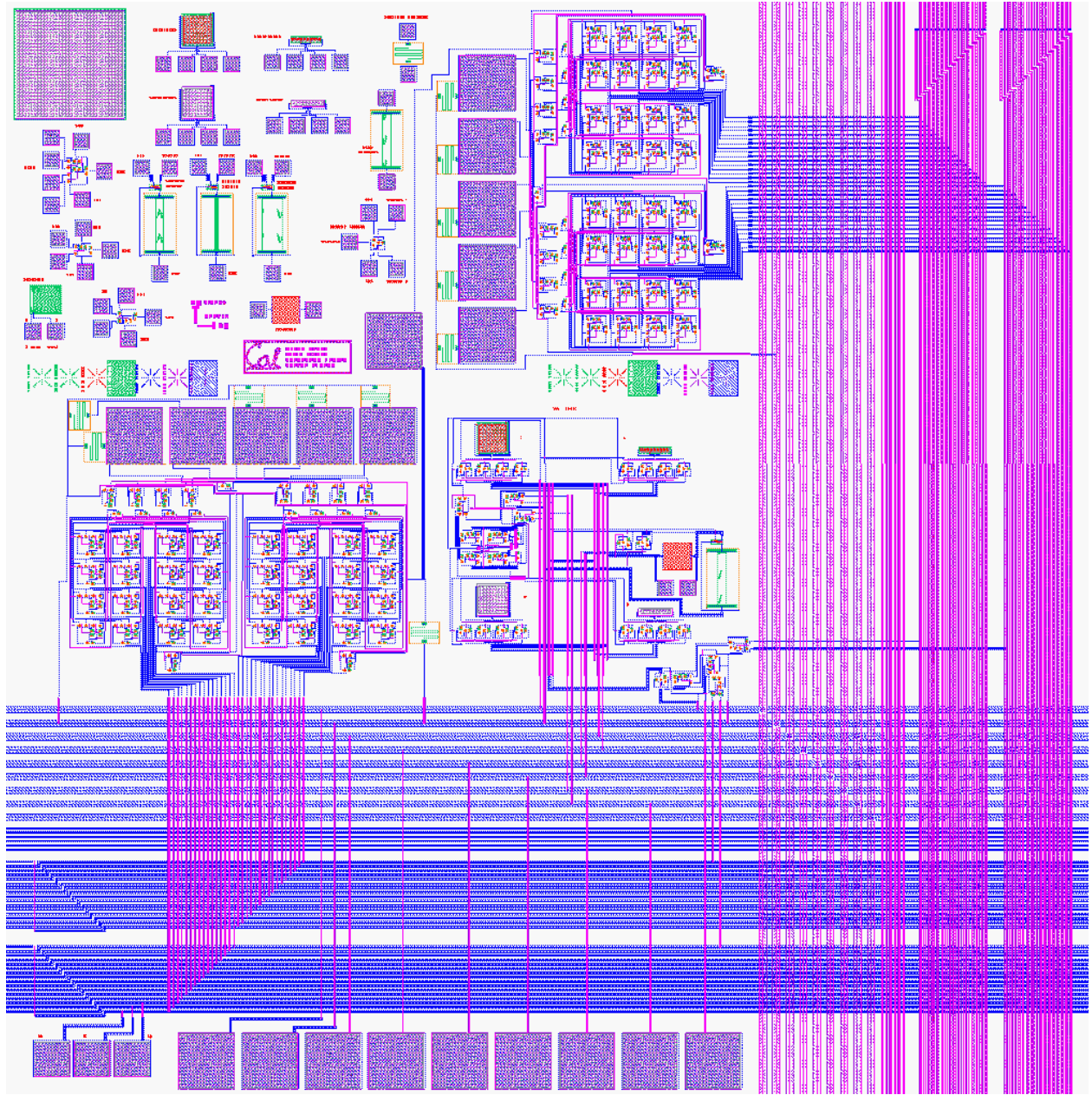


Figure 5.9: Full CMOS layout of etch-rate sensor.

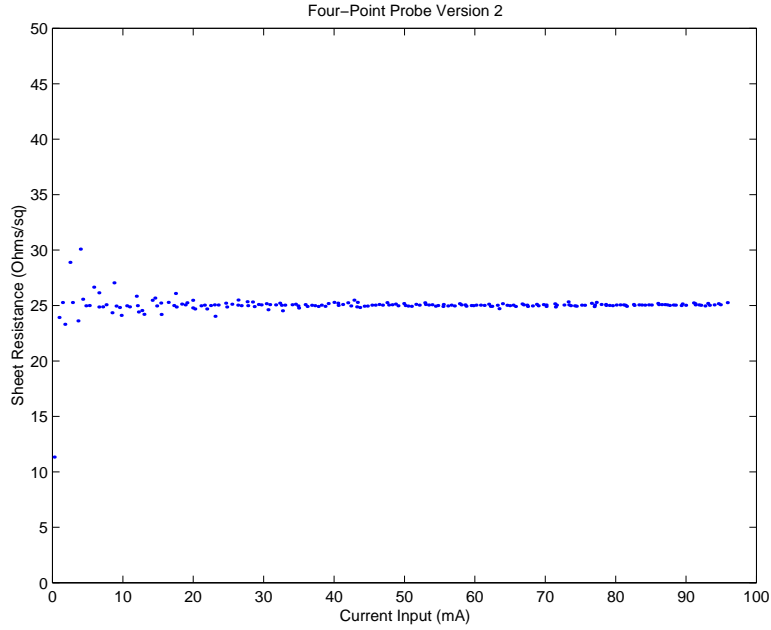


Figure 5.10: Plot of measured sheet resistivity vs. applied current

the right. The very top-left of the layout has a number of test structures, for diagnosis of problems on the fabricated wafer. Included with these test structures are one of each sensor geometry, with bond-pads attached directly to each of the four probe points.

5.2 Test Results

5.2.1 Bench Test

To test the sensor structure implemented with this design, one of the test-structure versions of the four-point probe was used. This test structure version, as described above, was simply a four-point probe with contact pads attached directly to each of the probes. A probe-station was used to make contact with the probes, and an external current source and voltmeter were used to interrogate the sensor. The current was scanned between $0mA$ and $100mA$, and the voltage was measured. The sheet resistance measurement, resulting from Equation 5.1, is plotted in Figure 5.10. From this graph it can be seen that the sheet resistance does not depend on current, as it did in the previous case, which indicates that this sensor is working. In addition, the externally measured sheet resistance of the polysilicon layer was $25 \frac{\Omega}{sq}$, which matches the sensor output very well.

The next step of the bench testing was to bond wires to the wafer using the techniques discussed in Section 4.2 and evaluate whether or not the multiplexing electronics were functional. This was performed (see Figure 5.11), and it was found that while the individual electronics worked, the overall circuit did not. Most likely, this was due to either a design flaw in the multiplexer

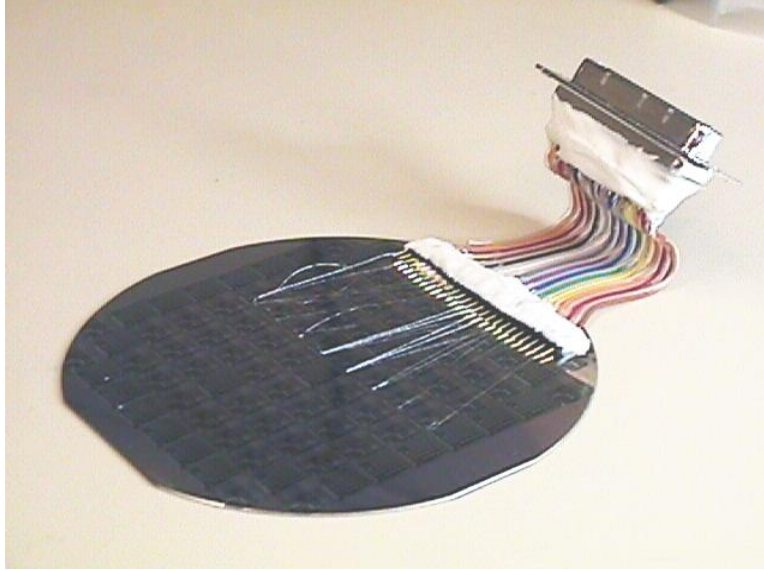


Figure 5.11: Picture of sensor wafer with wires attached.

circuitry, or a yield problem that rendered the multiplexers inoperable. However, because the individual (disconnected) sensors functioned well, the decision was made to wirebond directly to the sensors, and bypass the electronics. This was performed, and measurements were able to be made from eight sensors simultaneously. In order to be able to connect this many sensors to the limited number of available wires, the current-source pins of the sensors were wired together in series, so that the same current passed through all eight sensors. The induced voltages from each sensor were individually sensed.

5.2.2 XeF₂ Test

The XeF₂ etch chamber is a very simple structure, consisting of a small XeF₂ source bottle, an expansion chamber for collecting a volume of XeF₂ gas, a processing chamber, and a vacuum system. Three pneumatic valves control the flow of gas: V3 is between the XeF₂ source bottle and the expansion chamber, V1 is between the expansion chamber and the processing chamber, and V2 is between the processing chamber and the vacuum pump. To perform an etch, the three valves are controlled in such a way as to introduce a volume of XeF₂ gas into the chamber, let it sit for a period of time (typically ≈ 15 seconds), and pump it back out. The processing chamber is a circular aluminum dish with a clear Plexiglas lid.

Once the wires were bonded to the wafer, an electrical feedthrough was built into the Plexiglas lid of the XeF₂ etcher, so that the wires could be passed into the processing chamber. A **National Instruments AT-MIO/64-E3** data acquisition system was connected to the wafer so that automated measurements could be made and recorded. This setup is shown in Figure 5.12.

This system was attached to the XeF₂ etch chamber, and an etch experiment was carried



Figure 5.12: Picture of data acquisition system, including clear XeF_2 lid with electrical vacuum feedthrough.

out. The desired experimental procedure was as follows:

- ◇ Measure the thickness of each sensor using the NanoSpec /AFT reflectometric film-thickness measurement station.
- ◇ Record real-time measurements of film-thickness from the sensors, while performing a polysilicon etch in the XeF_2 reactor. Etch only $\approx 500 \text{ \AA}$ of the sensor film.
- ◇ Remove the sensor-wafer from the etch chamber and re-measure each sensor's new film-thickness using the NanoSpec.
- ◇ Compare readings from the sensors to the NanoSpec values.
- ◇ Repeat process until sensors are fully etched away (the total film thickness for these sensors is approximately 7000 \AA).
- ◇ Estimate the accuracy and precision of the sensors from these data

To control the etch-rate, the following procedure was used to regulate the flow of XeF_2 into and out of the etch chamber: V3 was opened for 30 seconds to allow a volume of XeF_2 gas to accumulate in the expansion chamber; V3 was closed and V1 was opened to begin the etch; after 15 seconds of etching, V2 was opened to pump out the etchant and byproducts. The first cycle of this experiment was conducted, and it was found that no etching occurred during the cycle (see Figure 5.13a). The reason for this is that XeF_2 etchant is highly selective to SiO_2 , and polysilicon

naturally forms a thin layer of native oxide. Therefore, it takes a long time for the XeF_2 to break through this SiO_2 layer. On the second etch cycle (shown in Figure 5.13b), the SiO_2 layer on the sensor closest to the XeF_2 input port was etched through, and the polysilicon etch proceeded at a very rapid pace. As can be seen from Figure 5.13b, the etch rate on the first sensor peaks out at over $3000 \frac{\text{\AA}}{\text{sec}}$. Because the etch sensors were only 4500 \AA to start with, the entire first sensor was consumed in a matter of roughly 2 seconds. In addition, because the sensors were wired in series, once the first sensor was destroyed all measurements ceased, although the sensors kept being etched. Therefore, although Figure 5.13b only appears to show the etching of a single sensor during etch cycle #2, in fact sensors #1,2,3,4, and 8 were completely consumed during this etch cycle. It was found that #5,6, and 7 were still functional, so the wirebonds were re-arranged to allow measurement of only these three sensors. To attempt to slow down the etch-rate, a small modification of the etch process was made: instead of keeping V3 open for 30 seconds to allow XeF_2 to accumulate in the expansion chamber, V3 was only kept open for 1 second, and an N_2 line was also opened into the expansion chamber for 7 seconds to dilute the XeF_2 gas. This etch cycle was performed (data shown in Figure 5.13c) on the remaining three sensors, and the etch-rate was still found to be much too high. The remaining three sensors were all consumed within 4 seconds.

While these data (Figure 5.13a 5.13b, and 5.13c) do show a measurement of something that looks like the proper film-thickness vs. time trend, no post-etch re-measurement could be performed. Therefore, the accuracy of the sensors could not be calculated. The decision was made to fabricate another test wafer, with features designed to overcome the problems encountered with this design.

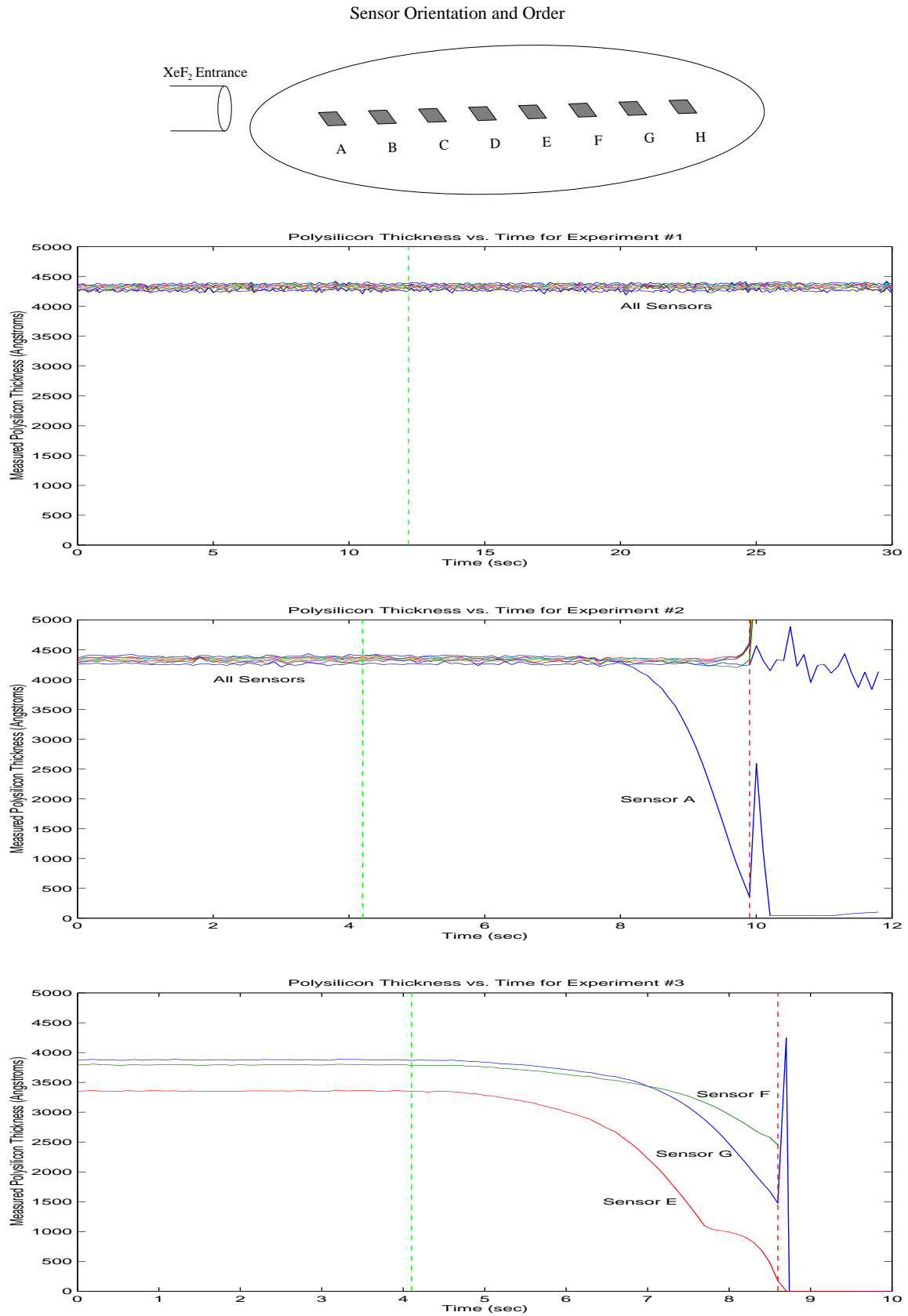


Figure 5.13: Data from *in-situ* etch experiments.

Chapter 6

Design III – Updated Sensor

6.1 Design Concept / Details

This sensor wafer utilizes the same sensor structure as the previous design (the van der Pauw probe), and the new design’s purpose is to eliminate or reduce the problems encountered in the testing phase of the second design. These problems are summarized in the list below.

- ◇ High etch rate eliminates the possibility of re-measurement of sensors
- ◇ Serial connection of sensors makes measurements stop once any sensor is etched through
- ◇ The one-year time between design and experiment makes correction of problems difficult.

The first problem, the high etch-rate, was mainly due to the very low open-area of the second design. On each 0.64cm^2 die, only $\approx 8.5 \times 10^{-4}\text{cm}^2$ was taken up by exposed polysilicon, which is an open area ratio of about 0.13%. Therefore, the etchant was not “loaded-down” by etch byproducts, and the etch proceeded at a very rapid rate. This problem was solved in the new design through the use of a “guard-ring” of polysilicon around the edge of the wafer. This extra band of polysilicon serves to increase the open area to around 50%, loading-down the XeF_2 reactor and reducing the etch-rate dramatically. This guard-ring can be seen in Figure 6.1.

The problem with the serial connection of sensors is that if one sensor gets destroyed, all measurements from the other dies stop, due to the broken power connection. The benefit of a serial connection is a reduction in the number of required connector pins, because two pins can serve to supply power to any number of sensors. In the new design, the sensors are connected in parallel, which effectively doubles the required number of connector pins, as each sensor now requires four connections instead of only two. This problem is mediated by the use of surface-mounted multiplexer chips, which allow the connection of a number of sensors to relatively fewer connector

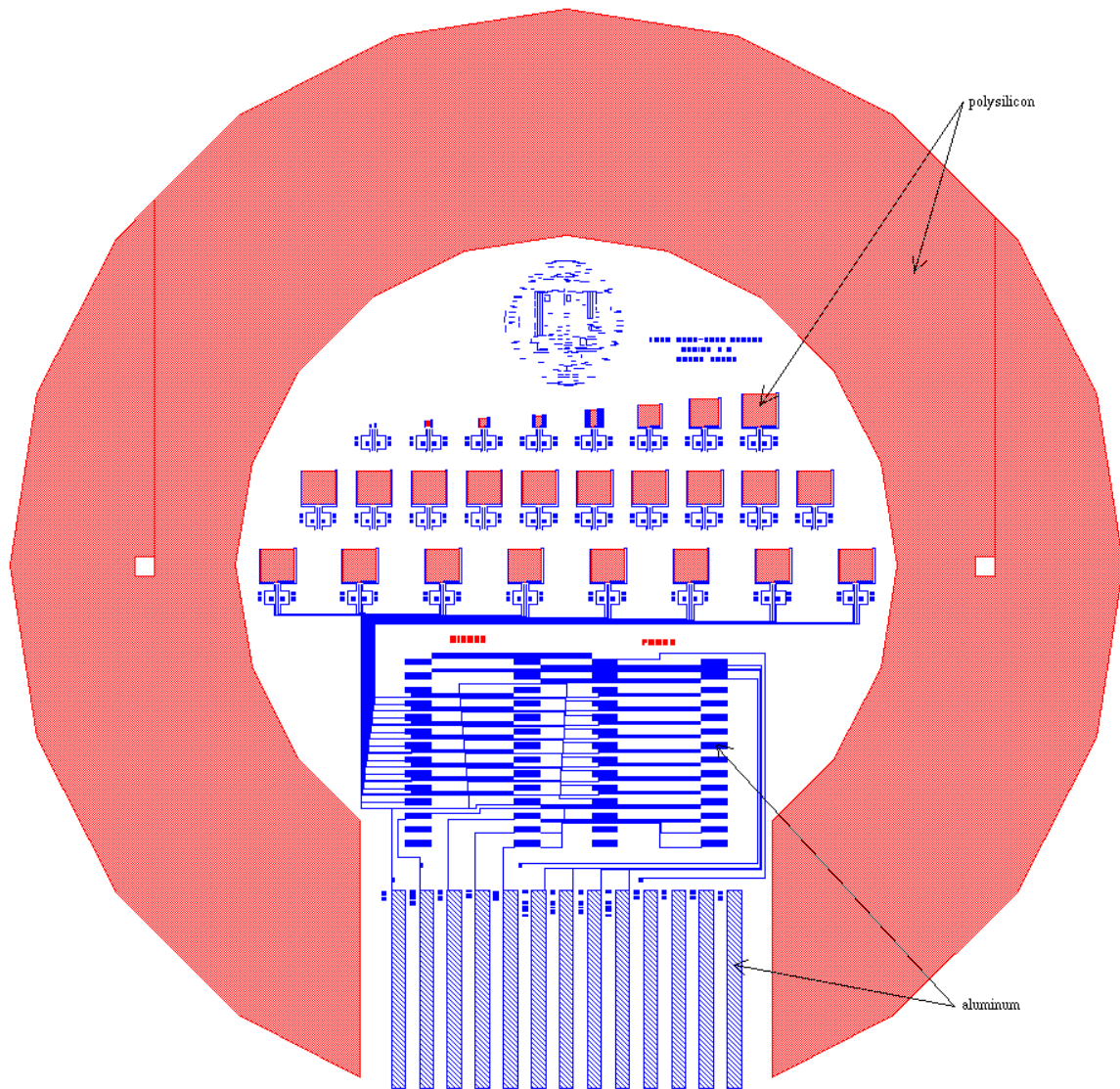


Figure 6.1: Layout of the third design. Polysilicon is red, aluminum is blue.

pins. The multiplexers used in this design are **Maxim MAX307** dual 8 input multiplexers, which allow the connection of 8 double-ended sensor outputs or power inputs to a single pair of connector pins. Address pins then allow the selection of a single sensor at a time. These chips are glued to the surface of the wafer in the proper position (with their pins touching the two rows of ten surface-mount aluminum pads, see Figure 6.1), and silver paint is used to make electrical connections to the wafer. Silver paint is a liquid paint that contains silver particles in a solvent base. When the solvent evaporates, the silver particles pack together, forming a conducting solid.

To reduce the time it takes to go from design to finished wafer, a much more simplified process was chosen, and several features were chosen to help speed up the time-to-experiment. First, the process only consists of two mask steps: a polysilicon patterning step to define the sensor pads, and a metal patterning step to define the interconnection wires. The entire process took two weeks, as opposed to the one year processing time required for the second design. Because this process did not allow any active devices (transistors) to be fabricated, all electronics had to be mounted on the surface, as described above. Another feature added to speed up the time-to-experiment is the way in which electrical connections are made to the wafer. In the previous design, a tedious gluing process was used, which typically took about three days due to the long glue-drying time. In this design, an “edge-board connector” was used to make connections to metal strips that run to the edge of the wafer at the flat. An edge-board connector is typically used to make connections to printed circuit boards, as in desktop computer ISA slots. In this way, to make connections to the wafer, all that is necessary is to slide on the connector, aligning the pins of the connector with the metal strips on the wafer (see Figure 6.2). These metal strips can be seen at the bottom of the layout in Figure 6.1.

6.2 Test Results

6.2.1 Test Procedure

Once the wafers were completed, the multiplexer chips were glued to a wafer, and an attempt was made to silver paint the connections. Problems were encountered on the left side of the left multiplexer, due to the thin wires that run between the surface-mount pads. Because the silver paint tends to spread out upon application, it was virtually impossible to paint all fifty-six connections without overlapping any of the thin wires. Any short between one of the pads and the wires caused a failure of at least one sensor, and possibly the entire wafer. This difficulty led to the decision to eliminate the multiplexers and simply wirebond between the edge-board pads and three of the sensors, so that direct measurement could be carried out. This was performed, and the edge-board connector was attached (see Figure 6.2), so that electrical tests could be performed. These electrical tests showed that all three sensors gave readings which agreed with the measured

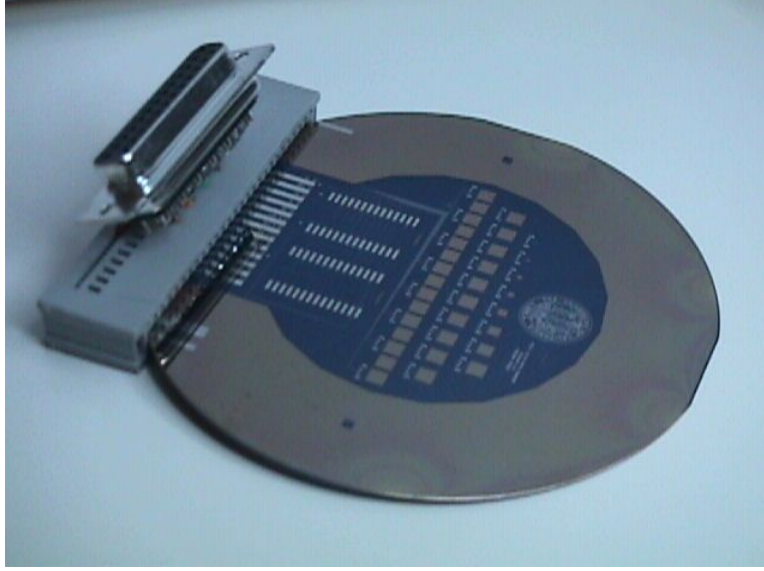


Figure 6.2: Picture of third sensor wafer design, with edge-board connector attached

sheet resistances.

6.2.2 XeF₂ Test

Testing was carried out in the same manner as described in Section 5.2.2, and all of the data is shown in Figures 6.3, 6.4, 6.5, and 6.6. The first five etch cycles yielded no measured change in film-thickness, and this can be attributed to the high selectivity of XeF₂ etchant to SiO₂. Because polysilicon slowly grows a thin layer of native SiO₂ on its surface, the beginning of the etch process proceeds very slowly while this SiO₂ is being etched away. Then, once the etchant breaks through the SiO₂ layer, the polysilicon etch proceeds rapidly. This begins to occur in experiment #7.

One problem that was observed was that because the selectivity of XeF₂ to SiO₂ is so high, the surface of an etched polysilicon film tends to become very rough. This is because as the etchant begins to break through the SiO₂ layer in some parts, the polysilicon etch occurs rapidly at these points, but not at the other parts of the surface that are still covered by SiO₂. Therefore, deep pits develop in the surface, contributing to a surface roughness on the order of 1000 Å. A surface roughness on this order makes the results from the reflectometry measurement meaningless, due to the scattering effects of roughness. Therefore, the results of the NanoSpec measurement (shown in Table 6.1) for thicknesses below about 6100 Å should be disregarded. Above this point, it is possible that the NanoSpec results are somewhat accurate due to the limited amount of etching that has taken place, but they are still not as accurate as for a flat film surface.

Another phenomenon that was noticed in the experimental results is the temperature sensitivity of the polysilicon sensor pads. Heavily doped semiconductors exhibit an increase in resistivity with increasing temperature, due to the decreasing carrier mobility[16]. This increase in resistivity,

Sensor Orientation and Order

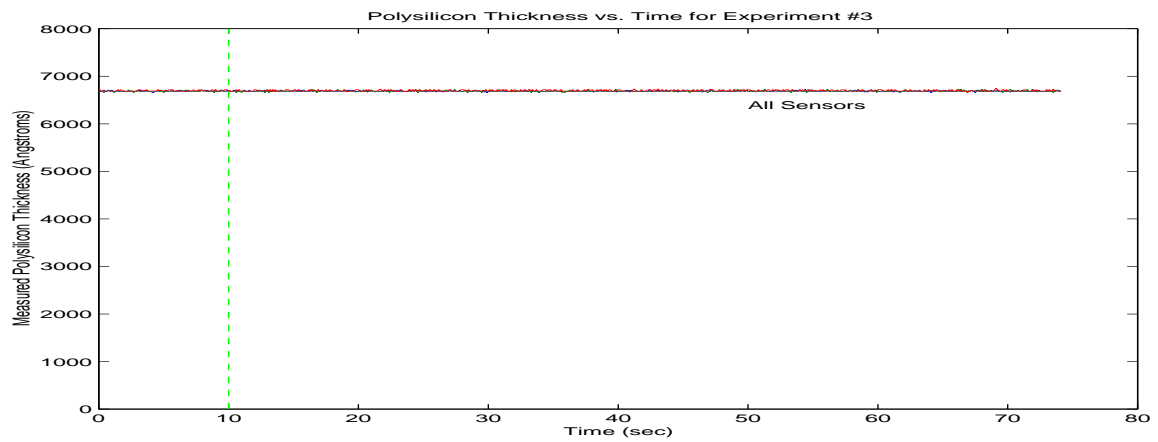
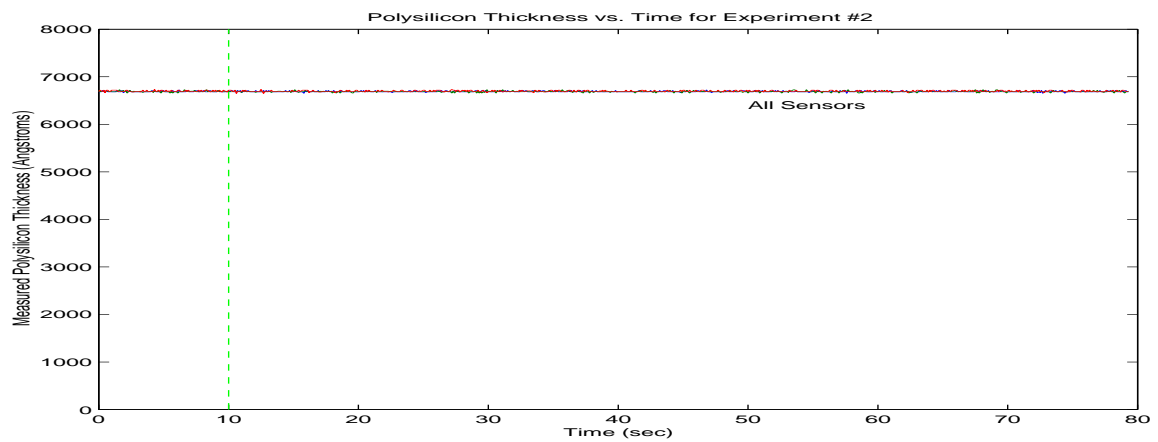
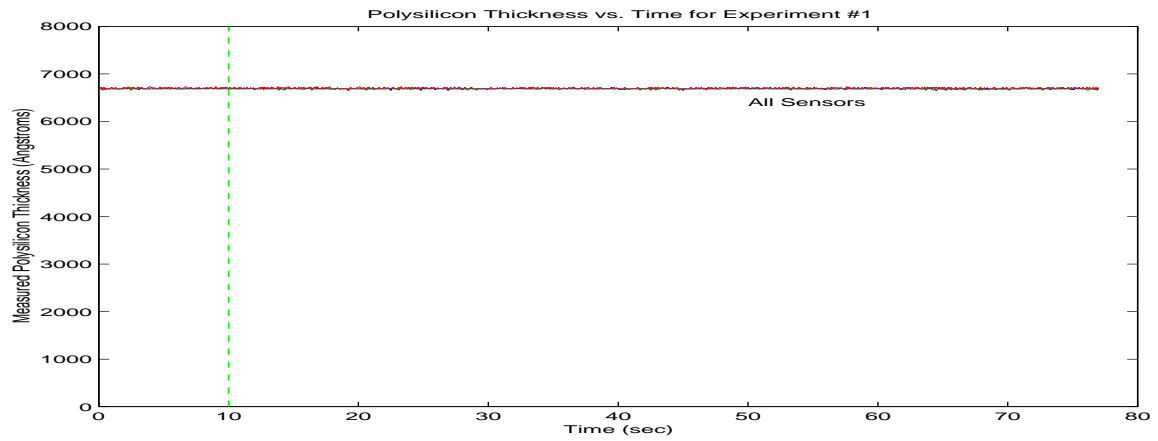
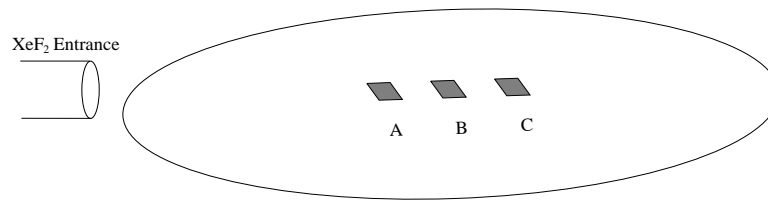


Figure 6.3: Experimental results from experiments 1-3

Sensor Orientation and Order

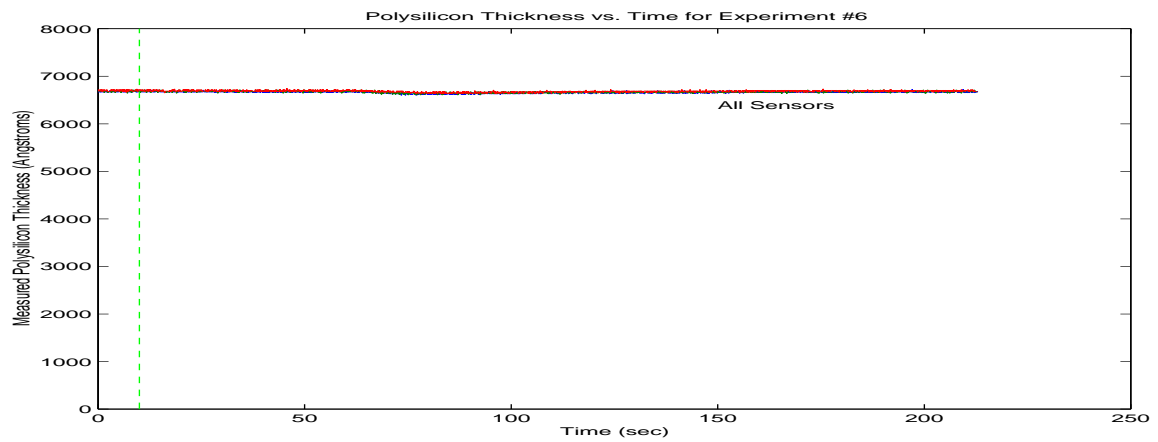
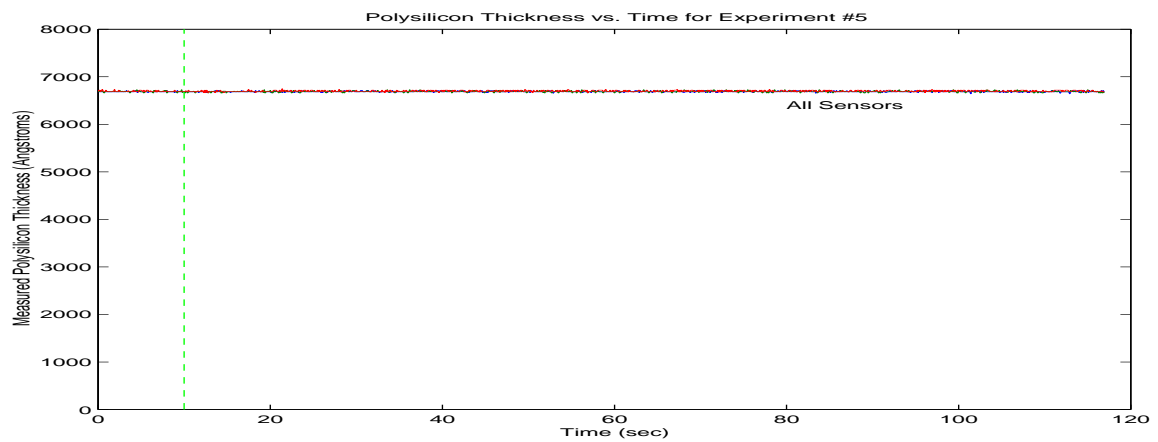
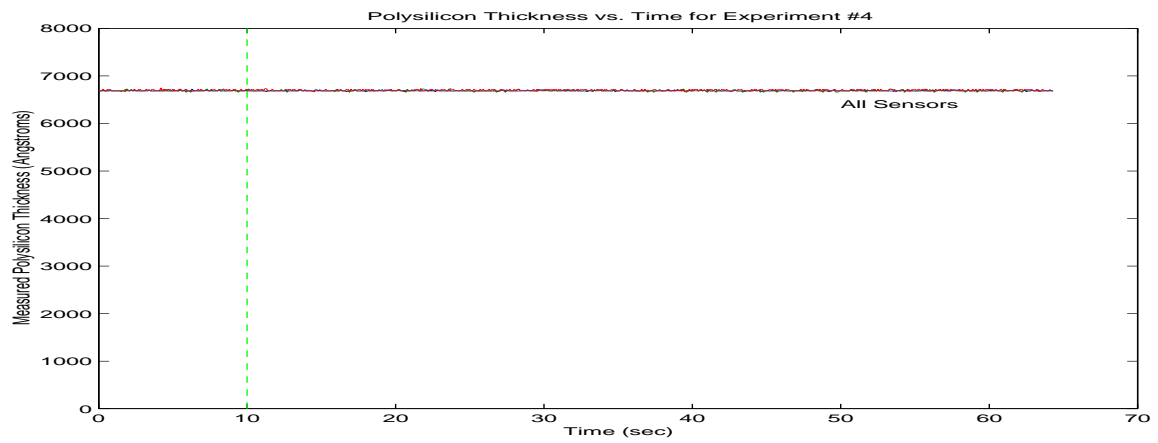
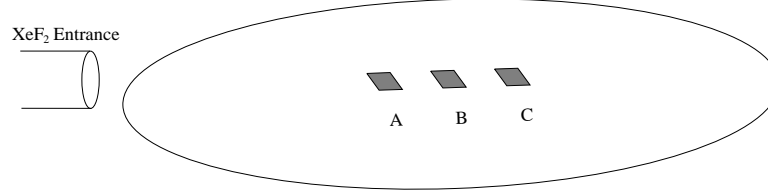


Figure 6.4: Experimental results from experiments 4-6

Sensor Orientation and Order

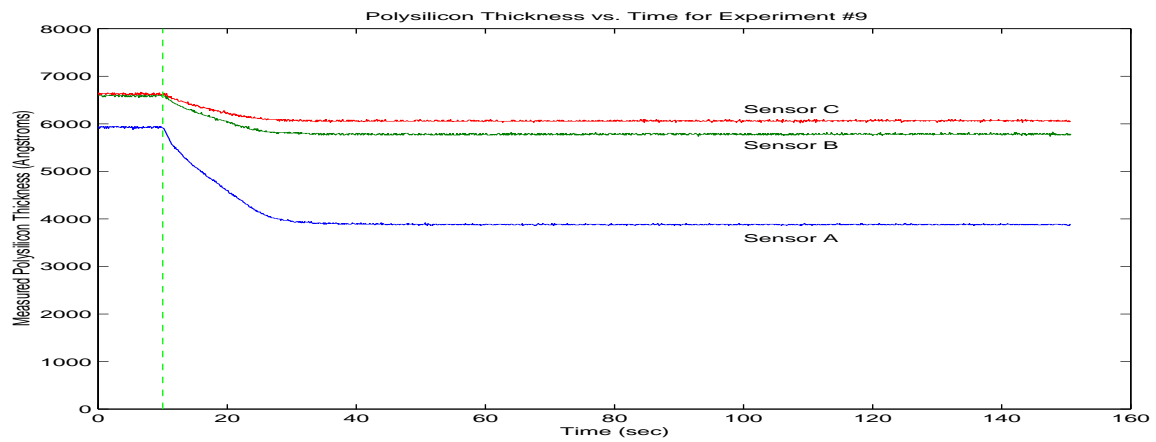
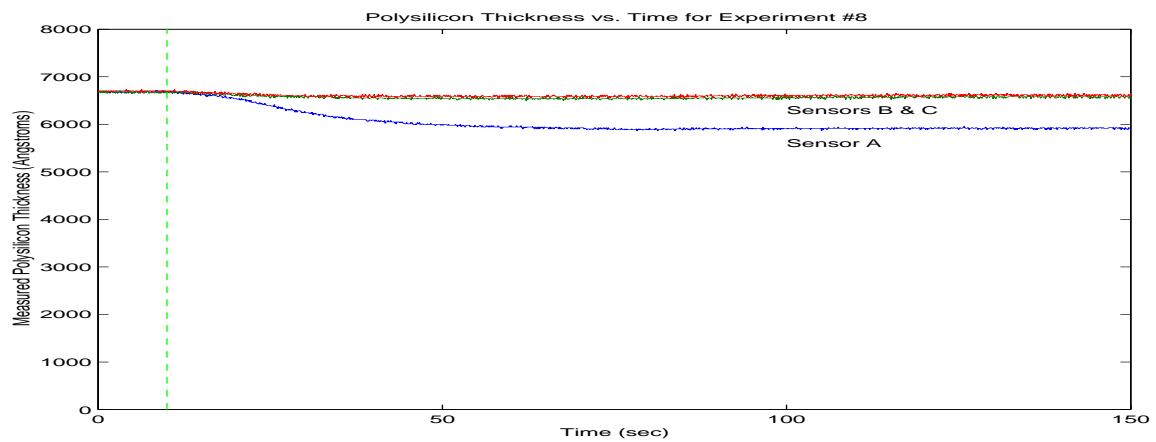
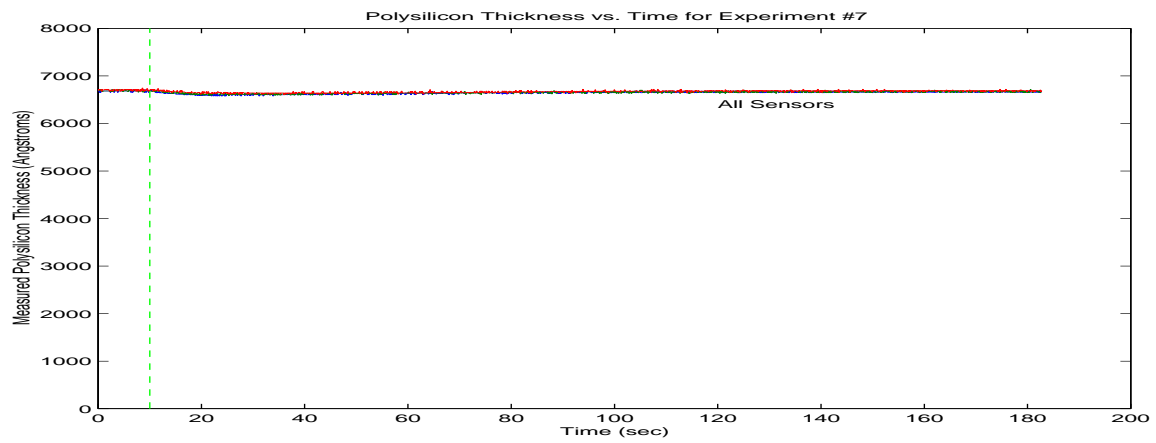
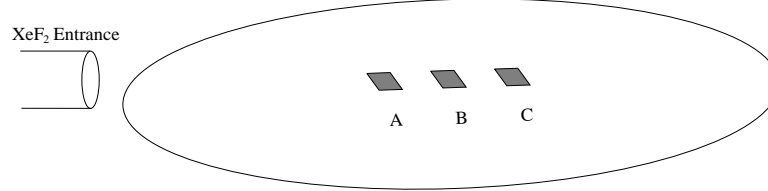


Figure 6.5: Experimental results from experiments 7-9

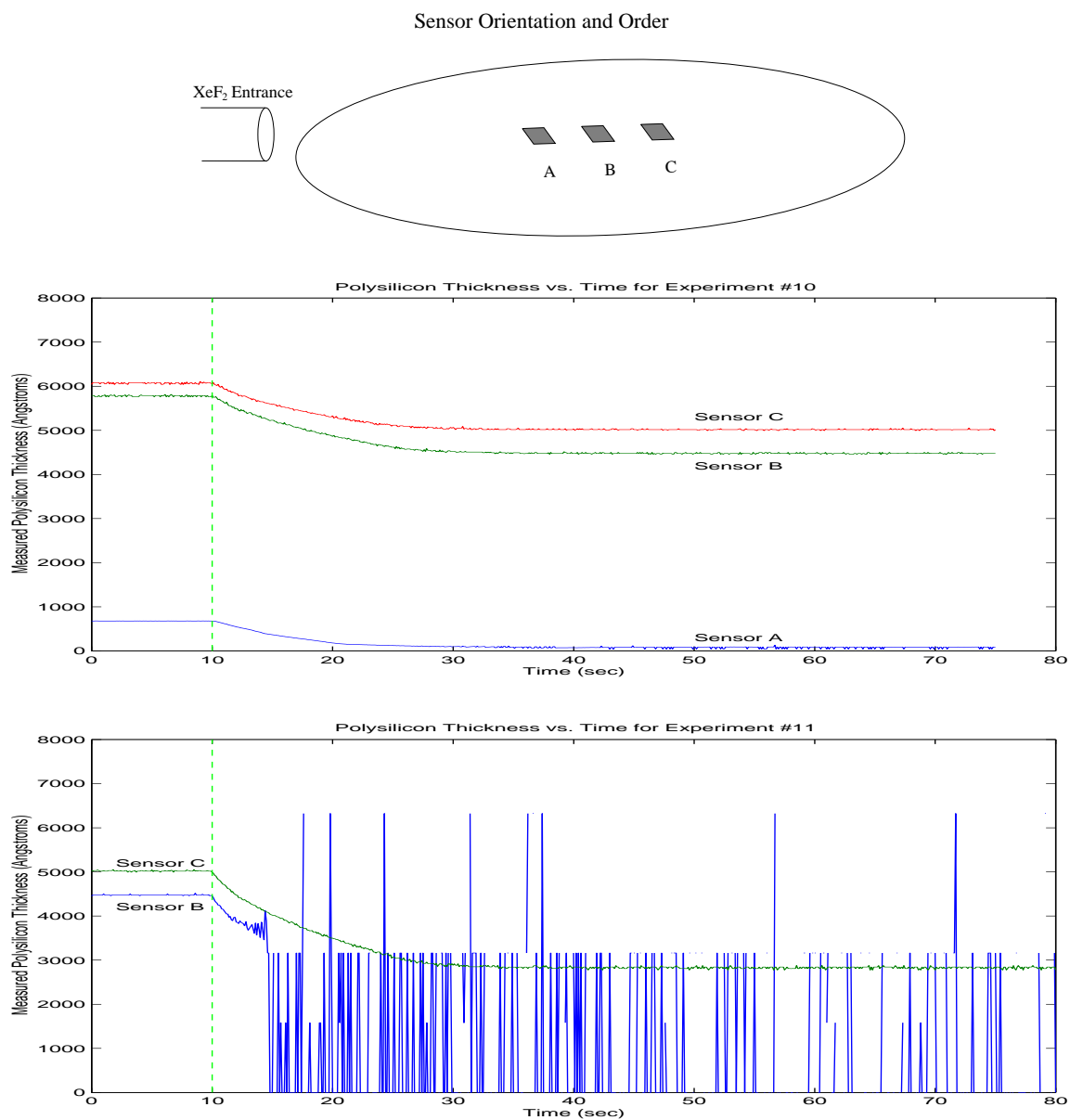


Figure 6.6: Experimental results from experiments 10-11

Trial		Sensor Measurement		NanoSpec	
Experiment #	Sensor #	Average (\AA)	St. Dev. (\AA)	Measurement (\AA)	Bias (\AA)
1	1	6689.1	12.5497	6686.0	3.1
	2	6691.2	12.3847	6687.3	3.9
	3	6700.9	14.4475	6696.7	4.2
6	1	6677.4	13.1019	6691.7	-14.3
	2	6685.6	10.4487	6692.0	-6.4
	3	6699.0	14.8000	6698.0	1.0
7	1	6682.9	12.1434	6689.7	-6.8
	2	6689.8	12.9128	6692.3	-2.5
	3	6704.0	14.1274	6699.0	5.0
8	1	6679.1	10.9611	6663.7	15.4
	2	6678.3	15.3468	6668.0	10.3
	3	6698.6	13.1639	6682.0	16.6
9	1	5925.1	13.7359	6417.4	N/A
	2	6586.5	13.2248	6632.4	-45.9
	3	6623.1	14.9344	6650.6	-27.5
10	1	678.4	0.7725	N/A	N/A
	2	5782.3	13.0169	6416.6	N/A
	3	6069.7	13.6125	6537.0	N/A
11	1	N/A	N/A	N/A	N/A
	2	4477.1	8.4099	N/A	N/A
	3	5022.1	10.5909	6309.0	N/A

Table 6.1: Results of sensor and NanoSpec measurements

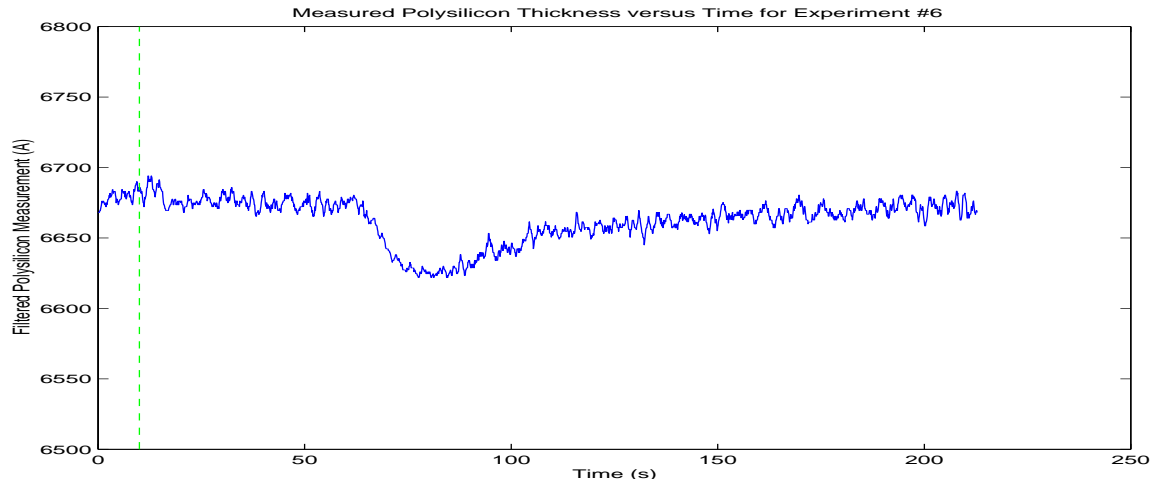


Figure 6.7: Blowup of experiment #5, showing dip in thickness due to temperature rise

in the absence of a film-thickness change, could be interpreted as a loss of thickness (due to the entry of ρ in Equation 5.2). In experiment #6, a slight dip in measured thickness occurs at around 50 seconds after the etch begins (see Figure 6.7 for a close-up). This dip is due to a rise in temperature due to the beginning of etching at the far edge of the wafer. Because the reaction of XeF_2 with silicon is highly exothermic, once the oxide breaks through on the edge of the wafer and the silicon begins to be etched, the temperature of the entire wafer goes up by about $10\text{-}20^\circ\text{C}$. It is this shift that is being measured in experiment #6. While this is detrimental to the thickness measurement because it confounds two quantities (film-thickness and temperature) in the same measurement, it opens the possibility of using this sensor, isolated from the environment by an oxide layer, to measure temperature. If it is to be used to measure film-thickness, then a buried sensor should be placed next to the exposed sensor, and the readings from the buried sensor should be used to calibrate out the temperature shift.

6.2.3 Analysis of Results

Table 6.1 summarizes all of the experimental results, with comparisons of the sensor measurements to the NanoSpec measurements. Based on these data, the accuracy, repeatability, linearity, and stability of the sensor can be estimated. First, it should be noted that the bias values are only listed in Table 6.1 for those rows that have a sensor-measured thickness greater than 6100 \AA . Even with this restriction, the NanoSpec-measured thicknesses above this limit are still questionable; therefore, the accuracy results quoted below should be interpreted in this context.

By averaging the available bias values from Table 6.1, the average bias of the sensor comes out to -3.1 \AA . It should be noted that as the sensor thickness goes down, this bias also goes down, possibly indicating errors in the NanoSpec measurement. The maximum observed bias is -45.9 \AA ,

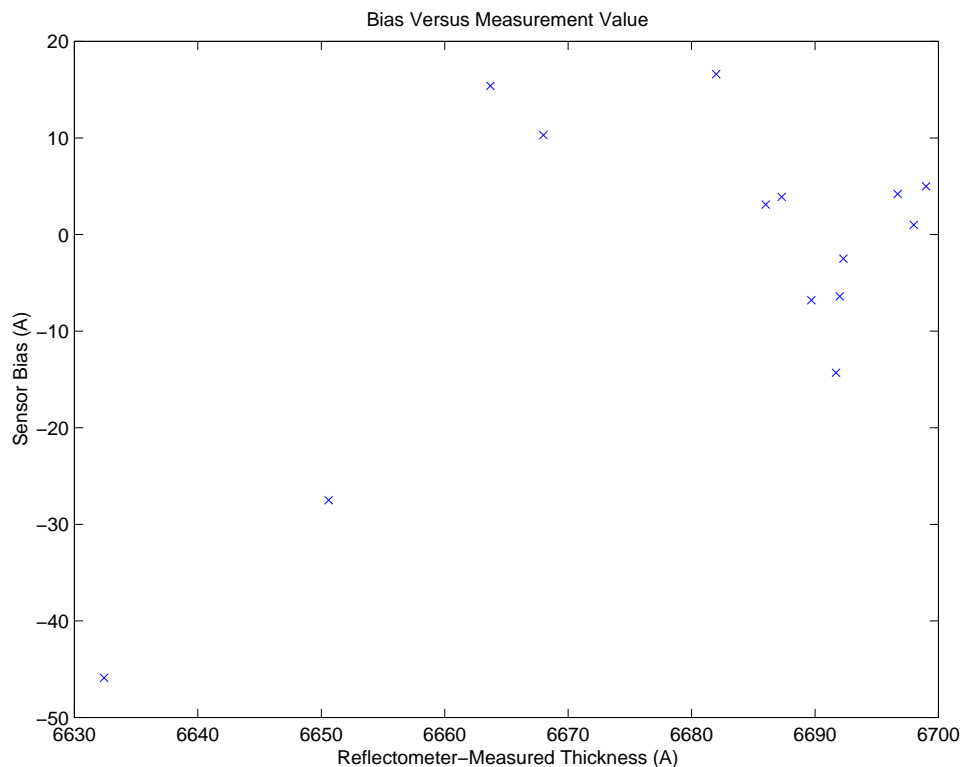


Figure 6.8: Linearity of accuracy

which corresponds to a 0.7% error.

The repeatability of the sensor can be found by finding the standard deviation of a set of data for which the actual film-thickness is not changing. Since the film was not etched until experiment #7, the first data set (from experiment #1) can be used for this purpose. By averaging the repeatability of each of the sensors in experiment #1, the repeatability of the sensor is found to be 13.1 Å. This corresponds to 0.2% of the full-scale value. The most likely sources of this noise are electrical line noise and digitization noise. Because long ($\approx 1.5\text{m}$) cables connect the sensor to the A/D converter of the computer, noise is injected by E/M fields in the area. Also, the inherent quantization of the A/D converter further adds noise to the measurement.

To assess the linearity of accuracy for this sensor, a plot of the bias versus NanoSpec-measured thickness is made (see Figure 6.8). From the plot, it appears that the accuracy is fairly constant over the thickness range plotted. However, there are a few complicating factors. First, because of the NanoSpec measurement problem, the range of thickness plotted on the graph is very narrow, which limits the evaluation of linearity. Second, the two points at the lower-left corner of the graph are from thinner polysilicon samples. Therefore, they could be becoming inaccurate as a result of the surface roughening effect described above. Therefore, the linearity of accuracy is still relatively unknown based on these data.

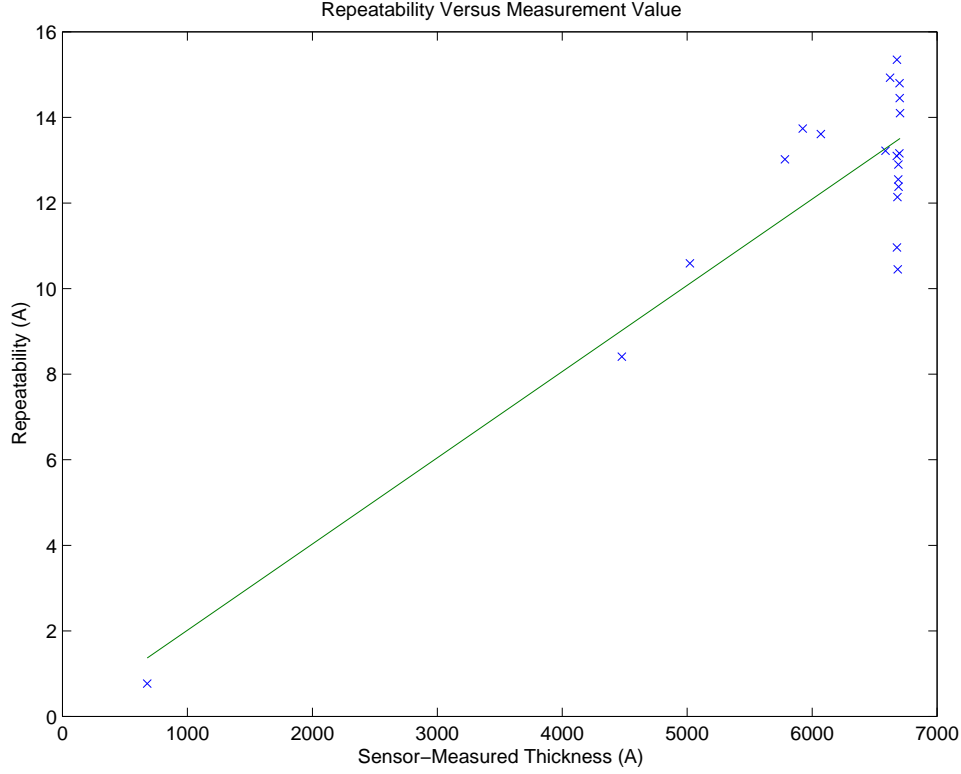


Figure 6.9: Linearity of repeatability

The linearity of repeatability is a less difficult calculation to make, because the NanoSpec measurement does not play a role. The repeatabilities of each sensor measurement (taken from Table 6.1) are plotted versus sensor-measured thickness in Figure 6.9. This figure shows an interesting trend at lower thicknesses. It appears that a regression line can be fit to the data, which would indicate that the repeatability gets better as the thickness goes down. This can be explained by examining the propagation of error in the calculation of thickness from voltage and current measurements:

$$\sigma_{\text{thickness}}^2 = \frac{\ln 2}{\pi} \rho \left[\frac{1}{V} \sigma_I^2 + \frac{I}{V^2} \sigma_V^2 \right] \quad (6.1)$$

where σ_I^2 is the variance of the current measurements and σ_V^2 is the variance of the voltage measurements. It can be seen from Equation 6.1 that as the voltage goes up and the current drops (as happens when the film is getting thinner), the variance of the thickness goes down nearly linearly. However, because the repeatability is going down linearly with thickness, the percentage repeatability stays constant, which means that the measurement does not really get any better at low thicknesses.

The stability of the sensor can only be evaluated over a time scale of several minutes, due to the limited data available. Because the actual film-thickness did not change between the beginning

of experiment #1 and the end of experiment #5, the entire set of data between these two points can be used to check for drifts in the sensor output. The average value of the first 30 seconds of data from experiment #1 is 6689.1 Å, while the last 30 seconds of data from experiment #5 is 6685.9 Å. The time span between these values is approximately 15 minutes. Therefore, the sensor output drifted down by 3.2 Å in 15 minutes. This small drift could easily be attributed to changes in the temperature of the wafer, as polysilicon resistivity depends heavily on temperature.

Chapter 7

Conclusions

In-Situ on-wafer sensors could be very beneficial to the semiconductor processing industry. There are a number of suitable applications for such a sensor, and the benefits afforded by these applications outweigh the costs. Given the results presented in this paper, it is possible to construct such a sensor wafer, and using the power, communication, and isolation techniques discussed, it might be possible to place one into a process chamber. Further work needs to be conducted into specific choices of power, communication, and isolation techniques, so that the techniques can be experimentally verified. Once these techniques are chosen and verified, a number of other sensor technologies can be easily tested and used.

Chapter 8

Acknowledgments

I would like to thank Professors Kameshwar Poolla and Costas Spanos for their generous assistance and good ideas during the course of this project. Thanks also to Guobin Wang, who pushed a full CMOS process through the UCB Microlab, and managed to get good devices on the other side. Scott Eitapence also deserves thanks, for fabricating one of the designs and thereby keeping me out of the Microlab for another few months. This work has been supported by the Department of Defense Graduate Research Fellowship, as well as UC SMART grant SM97-01.

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Appendix A

A.1 Four-Point Probe

The four-point probe technique can be used to measure sheet resistance (resistivity divided by thickness) of a thin sheet of material. According to this method, four small probes are placed on a planar sample of material in a straight line. In the ideal case, the sample must be an infinite plane. See Figure A.1 for a schematic of this arrangement. However, corrections can be made to the ideal case to allow for finite geometries.

To find a relation between the voltage measured and the current sourced, we first find the voltage at a point p , which is located at a distance r from a point current source (sourcing current I), in a very thin sheet of material. It is assumed that the material is much thinner than the probe spacing, so that no current flows in the vertical direction within the material. Because it is assumed that the current flows outward uniformly into the material, the current density can be found by dividing the total current by the area of a cylindrical surface centered about the source:

$$J = \frac{I}{(2\pi r) t} \quad (\text{A.1})$$

where J is the current density, t is the thickness of the sheet, and r is the distance from the current source. Now, voltage and current density are related by $-\nabla V = E = \rho J$, or in this one-dimensional case $-\frac{d}{dr}V = \rho J$, where ρ is the resistivity of the material. Solving this equation with J defined as

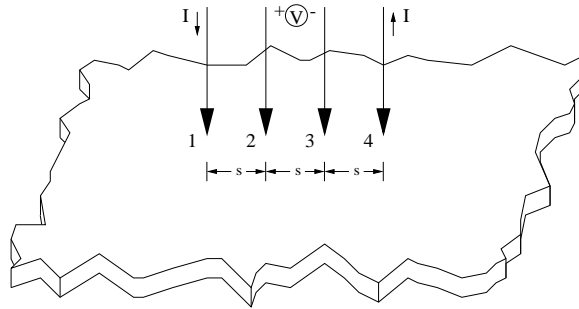


Figure A.1: Infinite sheet with linear four-probe arrangement

in Equation A.1 above yields:

$$V = -\frac{\rho I}{2\pi t} \ln(r) \quad (\text{A.2})$$

Applying this equation to the four-point probe situation, where there are both a current source (probe #1) *and* a current sink (probe #4), the voltages at the inner probes (probes #2 and #3) are:

$$V_2 = -\frac{\rho I}{2\pi t} \ln(s) - \frac{\rho(-I)}{2\pi t} \ln(2s) \quad (\text{A.3})$$

$$V_3 = -\frac{\rho I}{2\pi t} \ln(2s) - \frac{\rho(-I)}{2\pi t} \ln(s) \quad (\text{A.4})$$

Now, to find the voltage difference measured across probes #2 and #3, the two voltages are subtracted:

$$\begin{aligned} V_{diff} &= \left(-\frac{\rho I}{2\pi t} \ln(s) - \frac{\rho(-I)}{2\pi t} \ln(2s) \right) - \left(-\frac{\rho I}{2\pi t} \ln(2s) - \frac{\rho(-I)}{2\pi t} \ln(s) \right) \\ &= \frac{\rho I}{2\pi t} (2 \ln(2s) - 2 \ln(s)) \\ &= \frac{\rho I}{\pi t} \ln 2 \end{aligned} \quad (\text{A.5})$$

Finally, solving this equation for $\frac{\rho}{t}$, the sheet-resistance, yields:

$$\rho_s \equiv \frac{\rho}{t} = \frac{\pi}{\ln 2} \frac{V}{I} \quad (\text{A.6})$$

This result only applies to the ideal infinite plane case. However, it has been shown by L. Valdes that a correction factor F can be added to Equation A.6 which corrects the equation for non-infinite geometry[17]:

$$\rho_s = F \frac{\pi}{\ln 2} \frac{V}{I} \quad (\text{A.7})$$

The dimensionless parameter F is a function of geometrical factors including sample size and probe placement relative to sample edges, and can be calculated using a number of methods[14]. However, if the lateral diameter of the sample is much larger (at least a factor of 10) than the probe spacing, and if the probe spacing is much larger than the sample thickness, then F is very close to unity[17].

A.2 UC Berkeley Baseline CMOS Process Flow

Microlab CMOS Process
Version 5.0 (Nov. 1997)
1.3 μm , twin-well, double poly-Si, double metal

- 0.0 Starting Wafers: 24-36 $\Omega\text{-cm}$, p-type, <100>
Control wafers: PCH, NCH.
Scribe lot and wafer number on each wafer, including controls.
Piranha clean and dip in sink8.
Measure bulk resistivity ($\Omega\text{-cm}$) of each on sonogage.
- 1.0 Initial Oxidation: target = 30 ($\pm 5\%$) nm
 - 1.1 TCA clean furnace tube (tylan5), reserve tylan9.
 - 1.2 Standard clean wafers in sink6:
Include PCH and NCH.
piranha 10 minutes, 10/1 HF dip, spin-dry.
 - 1.3 Dry oxidation at 950 $^{\circ}\text{C}$ (SGATEOX):
60 min. dry O_2 (Check the previous run result)
20 min. dry N_2
measure oxide thickness on PCH
- 2.0 Nitride Deposition (SNITC):
Transfer wafers to tylan9 right after dry oxidation and deposit
Only include NCH.
100 nm nitride.
measure nitride thickness on NCH
- 3.0 Well Photo: Mask NWELL (CWN chrome-df)
(Control wafers are not included in any photoresist step)
Standard I-line process:
HMDS, spin (and soft bake), expose, post exposure bake,
develop, inspect, descum and hard bake.
- 4.0 Etch: Plasma etch nitride in lam1.
Check the oxide thickness on each work wafer
- 5.0 N-Well Implant: phosphorus, $4 \times 10^{12}/\text{cm}^2$, 80 KeV. Include PCH.
- 6.0 N-Well Cover Oxidation:
 - 6.1 TCA clean furnace tube (tylan2).
 - 6.2 Remove PR in O_2 plasma and clean wafers in sink8.
 - 6.3 Standard clean wafers in sink6, include PCH and NCH.
 - 6.4 Well cover oxidation at 950 $^{\circ}\text{C}$ (NWELLCVR):
30 min. dry O_2
175 min. wet O_2
30 min. dry O_2
20 min. N_2
- 7.0 Nitride Removal, include NCH
 - 7.1 Dip in 10:1 BHF for 40 sec to remove thin oxide on top of Si_3N_4 .
 - 7.2 Etch nitride off in boiling phosphoric acid (sink7).
Measure T_{ox} in n-well on work wafers.
- 8.0 P-Well Implant: B11, $3 \times 10^{12}/\text{cm}^2$, 80 KeV. Include NCH

- 9.0 Well Drive-In:
 - 9.1 TCA clean furnace tube (tylan2).
 - 9.2 Standard clean wafers in sink8 and sink6. Include PCH and NCH.
 - 9.3 Well drive at 1120 °C (WELLDLDR):
 - 60 min. temperature ramp from 750 °C to 1120 °C
 - 240 min. dry O₂
 - 300 min. N₂
 - Measure oxide thickness on two control wafers.
 - 9.4 Strip oxide in 5:1 BHF.
 - Measure R_S on PCH and NCH.
- 10.0 Pad Oxidation/Nitride Deposition:
 - target = 30 (± 6) nm SiO₂ + 100 (± 10) nm Si₃N₄
 - 10.1 TCA clean furnace tube (tylan5). Reserve tylan9.
 - 10.2 Standard clean wafers. Include PCH, NCH.
 - 10.3 Dry oxidation at 950 °C (SGATEOX):
 - ≈1 hr. dry O₂
 - 30 min. dry N₂ anneal.
 - Measure the oxide thickness on NCH
 - 10.4 Deposit 100 (±10) nm of Si₃N₄ immediately (SNITC):
 - Only include PCH.
 - approx.time = 22 min., temp.= 800 °C.
 - Measure nitride thickness on PCH.
- 11.0 Active Area Photo: Mask ACTV (ACTV emulsion-cf)
 - Standard I-line process.
- 12.0 Nitride Etch:
 - Plasma etch nitride in lam1.
 - Measure Tox on each work wafer. (2 pnts measurement).
 - Do not remove PR. Inspect.
 - Measure PR thickness covering active area.
 - PR must be >800 nm. Hard bake again for >2hrs at 120 °C.
- 13.0 P-Well Field Implant Photo: Mask PFIELD (CWINI emulsion-cf)
 - (Reversed NWEELL mask)
 - Standard I-line process. (Second photo)
 - N-Well area is covered with PR.
- 14.0 P-Well Field Ion Implant: B11, 70 KeV, $1.5 \times 10^{13}/cm^2$.
- 15.0 N-Well Field Implant Photo: Mask NWEELL (CWN chrome-df)
 - 15.1 Remove PR in plasma O₂. Clean wafers in sink8.
 - 15.2 Standard I-line process.
- 16.0 N-Well Field Ion Implant: phosphorus, 40 KeV, $3 \times 10^{12}/cm^2$.
- 17.0 Locos Oxidation: target = 650 nm
 - 17.1 TCA clean furnace tube (tylan2).
 - 17.2 Remove PR in O₂ plasma and piranha clean wafers.
 - Standard clean wafers; dip in BHF 25:1 for 5-10 sec.
 - Include PCH, NCH.
 - 17.3 Wet oxidation at 950 °C (SWETOXB):
 - 5 min. dry O₂
 - 4 hrs. 40 min. wet O₂
 - 5 min. dry O₂
 - 20 min. N₂ anneal
 - Measured Tox on 3 work wafers.

- 18.0 Nitride Removal, include PCH.
- 18.1 Dip in 10:1 BHF for 60 sec to remove thin oxide on top of Si_3N_4 .
 - 18.2 Etch nitride off in phosphoric acid at 145°C (sink7).
- 19.0 Sacrificial Oxide: target = $20 (\pm 2)$ nm
- 19.1 TCA clean furnace tube (tylan5).
 - 19.2 Standard clean wafers, include NCH and PCH.
Dip in 10:1 BHF until PCH and NCH dewet.
 - 19.3 Dry oxidation at 950°C (SGATEOX):
 - 30 minutes dry O_2
 - 30 minutes N_2 anneal
 - Measure T_{ox} on PCH and NCH.
- 20.0 N-Channel Punchthrough and Threshold Adjustment Photo: Mask PFIELD (CWINI emulsion-cf). Standard I-line process.
- 21.0 N-Channel Punchthrough and Threshold Adjustment Implant. Include NCH.
- 1) B11, 120 KeV, $8 \times 10^{11}/\text{cm}^2$.
 - 2) B11, 30 KeV, $1.9 \times 10^{12}/\text{cm}^2$.
- 22.0 P-Channel Punchthrough and Threshold Adjustment Photo: Mask PVT (PVT chrome-df).
Remove PR in plasma O_2 and clean wafers in sink8.
Standard I-line process.
- 23.0 P-Channel Punchthrough and Threshold Adjustment Implant. Include PCH.
- 1) Phosphorus, 190 KeV, $1 \times 10^{12}/\text{cm}^2$,
 - 2) B11, 20 KeV, $2.4 \times 10^{12}/\text{cm}^2$.
- 24.0 Gate Oxidation/Poly-Si Deposition:
target = $20 (\pm 2.0)$ nm SiO_2 + $450 (\pm 40)$ nm poly-Si
- 24.1 TCA clean furnace tube (tylan5).
Reserve poly-Si deposition tube (tylan11).
 - 24.2 Standard clean wafers, include PCH, NCH,
 T_{ox} (prime P<100>), and one Tpoly1 monitoring wafers.
 - 24.3 Dip off sacrificial oxide in 10:1 HF
until NCH and PCH dewet (approx. 1 min).
 - 24.4 Dry oxidation at 950°C (SGATEOX):
 - 30 min dry O_2 (Check previous run result)
 - 30 min N_2 anneal.
 - 24.5 Immediately after oxidation deposit 450 nm of phos.doped
poly-Si (SDOPOLYI). Only include Tpoly1.
approx.time = 2 hr. 20 min., temp.= 610°C
(Check previous run result)
 - 24.6 Measurements
 - a) Measure oxide thickness on T_{ox} , PCH and NCH.
 - b) Measure D_{it} and Q_{ox} on T_{ox} .
 - c) Strip oxide from PCH and NCH, and measure the sheet resistivity.
 - d) Measure poly thickness on Tpoly1.
PCH and NCH proceed to step 27.2.
Tpoly1 proceeds to step 32.3.
- 25.0 Gate Definition: Mask POLY (emulsion-cf)
Standard I-Line process.
- 26.0 Plasma etch poly-Si

26.1 Etch poly in Lam4 (Recipe: 400):

26.2 Measure T_{ox} in S/D area of each work wafer (2 pnts measurement).

26.3 Measure channel length using $1.0\mu m$ gate.

27.0 Reoxidation and Capacitor Formation:
 (If no capacitor is requested, skip step 27 through 29.2.)

27.1 TCA clean furnace tube (tylan2). Reserve tylan12 and tylan11.

27.2 Standard clean wafers, including PCH, NCH, and two monitoring wafers, one for dry oxidation (Tpoly2) and one for LTO.
 From here on: only 10 sec dip in 25/1 H_2O/HF after piranha.

27.3 Dry oxidation at $900^\circ C$ (SDRYOXB):
 30 min dry O_2
 20 min N_2 anneal.
 Measure oxide thickness on Tpoly2:
 Tpoly2 proceeds to Step 27.5.
 PCH proceeds to Step 34 and NCH proceeds to Step 31.

27.4 1) Run a coating and monitoring LTO in tylan12 to get dep rate. Use recipe VDQLTOC and set 0 doping.
 2) Deposit LTO for the desired oxide thickness.
 3) Measure LTO thickness on monitoring wafer:

27.5 Second poly-Si deposition: immediately after oxidation deposit 450 nm of phos.doped poly-Si (SDOPOLYH):
 only include Tpoly2.
 approx.time = 2 hr. 18 min, temp. = $610^\circ C$.
 Measure second poly thickness on Tpoly2:
 Tpoly2 proceeds to step 32.3.

28.0 Capacitor Photo: Mask CAP-CE (CAP emulsion-cf)
 Standard I-Line process.

29.0 Plasma etch poly-Si:

29.1 Etch 2nd poly in Lam4 (Recipe: 400):

29.2 Measure T_{ox} in S/D area on each work wafer.
 Remove PR in O_2 plasma.
 Piranha clean wfrs in sink8.
 Dehydrate wfrs in oven for > 30 min. at $120^\circ C$.

30.0 N+ S/D Photo: Mask N+S/D (NSD chrome-df)
 Standard I-line process.

31.0 N+ S/D Implant: Arsenic, 100 keV, $5 \times 10^{15}/cm^2$, include NCH.

32.0 N+ S/D Anneal

32.1 TCA clean furnace tube (tylan7).

32.2 Remove PR in O_2 plasma and piranha clean wafers in sink8 (no dip here).

32.3 Standard clean wafers in sink6, incl. PCH, NCH, Tpoly1, and Tpoly2.

32.4 Anneal in N_2 at $900^\circ C$ for 30 min (N2ANNEAL).

32.5 Strip oxide from NCH, Tpoly1, and Tpoly2.
 Measure R_s of N+ S/D implant
 Measure R_s of poly1 on Tpoly1
 Measure R_s of poly2 on Tpoly2

33.0 P+ S/D Photo: Mask P+S/D (PSD emulsion-cf)
 Standard I-line process.

- 34.0 P+ S/D Implant: B11, 20 keV, $5 \times 10^{15}/\text{cm}^2$, include PCH.
- 35.0 PSG Deposition and Densification: target = 700 nm
- 35.1 Remove PR in O₂ plasma and clean wafers in sink8 (no dip).
 - 35.2 Standard clean wafers in sink6 (10 sec dip).
Include one PSG monitoring wafer.
 - 35.3 Deposit 700 nm PSG, PH3 flow at 10.3 sccm (SDOLTOD).
approx.time = 22 min. (check current dep. rate)
temp. = 450°C
 - 35.4 Densify glass in tytan2 at 900°C, immediately after
PSG deposition (PSGDENS). Include PSG control.
5 min dry O₂
20 min wet O₂
5 min dry O₂
Measure tPSG (using PSG control and working wafers):
Etch oxide on PCH.
Measure R_s of P+ S/D implant
 - 35.5 Do wet oxidation dummy run afterwards to clean tube:
1 hr wet oxidation at 950°C (SWETOXB).
- 36.0 Contact Photo: Mask CONT (CONT chrome-df)
Standard I-Line process.
- 37.0 Contact Plasma Etch in lam2:
- 38.0 Back side etch
- 38.1 Remove PR in O₂ plasma, piranha clean wafers in sink8 (no dip).
Dehydrate wafers in oven at 120°C for >30 min.
 - 38.2 Etch backside:
(PCH and NCH can be included in b), c) and d).
 - a) Spin PR on front side, hard bake.
 - b) Dip off oxide (PSG) in 5:1 BHF.
 - c) Etch poly-Si (poly2 thickness) in lam4.
 - d) Etch oxide off in 5:1 BHF (cap. ox. thickness).
 - e) Etch poly-Si (poly1 thickness) in lam1.
 - f) Final dip in BHF until back dewets.
 - g) Remove PR in PRS2000, piranha clean wfrs in sink8 (no dip).
- 39.0 Metallization: target = 600 nm
Std clean wfrs and do a 30 sec. 25/1 H₂O/HF dip just
before metallization.
Sputter Al/2% Si on all wafers in CPA.
- 40.0 Metal Photo: Mask METAL1-CM (M1 emulsion-cf)
Standard I-line process.
- 41.0 Plasma etch Al in Lam3.
Remove PR in PRS2000 or technics-c.
Probe test devices.
- 42.0 Sintering: 400°C for 20min in forming gas (tytan13).
No ramping, use SINT400 program.
- 43.0 Testing:
1.0 μm N- and P-channel devices, capacitors and inverter
Measure the sheet resistivities of PCH and
NCH on prometrix.
- 44.0 Planarization and Dielectric Film Deposition:

44.1 PECVD thin oxide (50 nm) in technics-B:
N₂O: 54.0, Silane: 14.0, Pwr: 15 W, Pressure: 360-420 mT.
≈5 min. Measure T_{ox} on dummy wafers.

44.2 SOG coating on the Headway spinner at 3000 rpm.

44.3 SOG cure:
a) Oven in Y2, 120°C, 30 min.
b) Oven in R1, 200°C, 30 min.
c) Tylan14 (SVANNEAL): 400°C, 30 min.
d) Measure T_{ox} and refractive index on dummy wafers.

44.4 ECR thick oxide (900 nm) in pqecr:
Check the deposition rate of previous run.
Measure T_{ox} and refractive index on dummy wafers.

45.0 VIA Photo: Mask VIA (VIA chrome-df)
Standard I-line process.

46.0 Etch VIA in lam2.
Need overetch.

47.0 Metal2 Metallization. target = 800-900 nm
Remove PR in PRS2000 or technics-c. Rinse the wafers in sink7 and spin dry.
Sputter Al/2% Si CPA.

48.0 Metal Photo: Mask METAL2-CM (M2 emulsion-cf)
Standard I-line process.
Hard bake for >2 hrs.

49.0 Plasma etch Al in Lam3.
Remove PR in PRS2000.

50.0 Sintering: 400°C for 20min in forming gas (tylan13).
No ramping, use SINT400 program.

51.0 Testing: Measure Metal1 and Metal2 contact chain.

End of Process