Autonomous Micro-sensor Arrays for Process Control of Semiconductor Manufacturing Processes[1]

Darin Fisher[ℏ], Mason Freed[◇], Costas Spanos[‡], and Kameshwar Poolla[†]

Abstract

In this paper we first motivate the use of autonomous micro-sensor arrays for use in semiconductor manufacturing. Following this, we discuss three critical issues that must be addressed in order to realize our goal of building these micro-sensor arrays. We then describe our on-going development efforts of fabricating spatially resolved etch-rate and temperature sensors.

1 Introduction

Over the past few years, the semiconductor processing industry has undergone a paradigm shift from *ex-situ* metrology to in-line metrology. Wafer measurement equipment has been moved, where possible, from stand-alone measurement stations to integrated measurement systems on or near the processing equipment. The benefits of this shift have been significant. Among the advantages of in line metrology are improved process monitoring, reduced product variance, and higher throughput. By placing the sensors on the equipment, *every* wafer is examined, as opposed to just a fraction, as is the case with stand-alone metrology stations. Because much more data is available, process fluctuations and trends can be much better characterized, monitored, and recorded. Also, the frequency of data availability make possible continual process adjustments as in run-to-run control, which result in reduced product variability. Finally, by measuring all of the wafers in-line and allowing them to continue instead of removing selected wafers for metrology, more production wafers can reach process completion, improving throughput.

[1]Supported in part by the National Science Foundation under Grant ECS-96-28420 and by UC SMART [S97-01].

[ℏ] Dept. of Mechanical Engineering, University of California, Berkeley CA 94720. Tel. (510)642-6152.
Email: `dfisher@jagger.me.berkeley.edu`

[◇] Dept. of Mechanical Engineering, University of California, Berkeley CA 94720. Tel. (510)642-6152.
Email: `mfreed@jagger.me.berkeley.edu`

[‡] Dept. of Electrical Engineering, University of California, Berkeley CA 94720. Tel. (510)643-5599.
Email: `spanos@bcam.eecs.berkeley.edu`

[†] Corresponding Author. Dept. of Mechanical Engineering, University of California, Berkeley CA 94720. Tel. (510)642-4642.
Email: `poolla@jagger.me.berkeley.edu`

While the benefits of in-line metrology are numerous, the money and time spent to integrate metrology stations onto equipment is not insignificant. In addition, equipment engineers are reluctant to modify existing equipment designs, to allow the addition of sensors and associated hardware, because such changes could adversely affect process stability, and this work is expensive. Also, if the metrology portion of the equipment goes down during production, the equipment must also be taken down to allow repairs to be performed, reducing the throughput of the machine. For these reasons, the next paradigm shift might be from sensors on the *equipment* to sensors on the *wafer*.

Such on-wafer sensor arrays can provide spatially and temporally resolved metrology about the wafer and process state with unprecedented resolution. This becomes possible at modest cost and without expensive equipment modifications. We envisage that these wireless sensor arrays could be loaded along with product wafers and sent into the processing chamber. During processing, the sensor-wafer would telemeter out (via RF, IR, or other wireless method) process state information. The most immediate use of these sensor-wafers is in the direction of process calibration, monitoring and control.

In this paper, we describe our on-going development of autonomous micro-sensor arrays. Our approach is two-fold. First, we are fabricating *component based sensor arrays* that employ surface-mounted off-the-shelf components. The focus here is on spatially resolved temperature metrology. Simultaneously, we are developing *fully integrated micro-sensor arrays* using baseline CMOS processing. The focus here is on spatially resolved etch-rate measurements.

The remainder of this paper is organized as follows. In Section 2, we discuss issues critical to the successful development of micro-sensor arrays for use in semiconductor manufacturing in general. Following this, Sections 3 and 4 detail our experiences with developing component-based and fully-integrated micro-sensor arrays respectively. We close with some concluding remarks in Section 5.

2 Sensor Design Issues

In creating an autonomous sensor wafer, several issues become important. These issues can be grouped into three main categories: power, communications, and isolation.

2.1 Power

An *in-situ* etch-rate sensor wafer must contain some type of wireless, regulated power source to provide power for the electronics and sensors. There are several constraints on such a power source. As stated, it must be wireless, because one of the major goals of this project is to construct a sensor wafer that "looks" as close to an actual product wafer as possible, to avoid problems with loading and unloading it from the chamber. This clearly precludes the use of wired connections to the wafer. Also, to avoid problems with wafer-handling robotics, the protrusion of the power source above the wafer surface must be limited to about 3mm. Another requirement for the power source is that it does not take up excessive area on the wafer. The smaller the power source, the more space is available for sensors. Lastly, the power source must be capable of supplying roughly 3V output, with a minimum of 1mA current, for at least 5 minutes. This is approximately the amount of power required to keep electronics and sensors running for the duration of the etch process (including loading and unloading).

Given these constraints, several power-supply opportunities exist. The primary candidates are battery-power, photovoltaic cells, and capacitive storage. Each method clearly has several advantages and disadvantages, with battery-power offering the most overall promise.

2.2 Communication

For an *in-situ* sensor wafer to be useful, the data it measures must be communicated to the outside world. Therefore, several restrictions exist for the sensor's communications system. First, the system must be capable of handling measurements from about 100 sensors, each operating at a minimum frequency of 1 Hz. Second, the measurements must be allowed at least 8 bits of precision, to enable accurate measurement data transmission. Therefore, the overall communications bandwidth must be at least $(100\,\text{sensors}) * (1\,\text{Hz}) * (8\,\text{bits}) = 800\,\text{Hz}$. Another requirement for the communications system is that it use very little power. Because the power source is only capable of delivering a limited amount of power, the communications system must use only a fraction of this amount. For the same reasons as for the power supply, the communications system must be wireless, and must fit within the same size constraints. Lastly, the communication system must not, as much as possible, depend on the particular geometry of the process-chamber. For example, if optical communications is used, the light-source must not be directed only toward the view port in a particular type of equipment, because then this sensor would be useless in other equipment in which the viewport is situated differently with respect to the wafer chuck.

For a multi-sensor wafer the communications can be either modular or central. For modular communication, each sensor (or possibly each group of sensors) would have its own communication system, so that the sensors transmit their data in parallel. With central communications, all of the sensors are connected to a central communications system, which communicates the data for the entire wafer. Different communications methodologies usually lend themselves more to one of these techniques than the other.

From the perspective of implementation, the simplest communications option is optical transmission. Other techniques, such as radio-frequency (RF) transmission and micromachined corner-cube retroreflector transmission are also possible.

2.3 Isolation

Because most of the processing techniques used in the semiconductor manufacturing industry place the wafers in "harsh" environments, any sensor that will be processed by the equipment needs to have some type of isolation from the environment. The main conditions that would be detrimental to a sensor wafer are high temperature and electrical noise. Also of importance are chemical attack and physical damage (such as etch damage).

In rapid thermal processing (RTP), for example, the temperature typically exceeds 1000 °C. Any electronics on the wafer that are not isolated will stop functioning above about 150 °C, and will melt at ≈ 550 °C (the aluminum interconnect melting temperature). Therefore, any sensor that might operate in this environment *must* be thermally shielded so that the electronics remain at a lower temperature.

In plasma-etch environments, the plasma is created by coupling radio-frequency (RF) power into a gas. Because of this high-power RF energy, surface currents are generated in exposed, unshielded conductors on the wafer surface. Therefore, if electronics are functioning on the wafer (as in the case of a sensor-wafer), then these generated currents might interfere. So a sensor wafer taking measurements inside a plasma chamber must be electrically isolated from the plasma environment to function properly.

One possible option to isolate the electronics and sensors from electrical noise is to add a metal layer over all of the electronics (but isolated by an oxide), and have a contact from this overcoat to the substrate. Also,

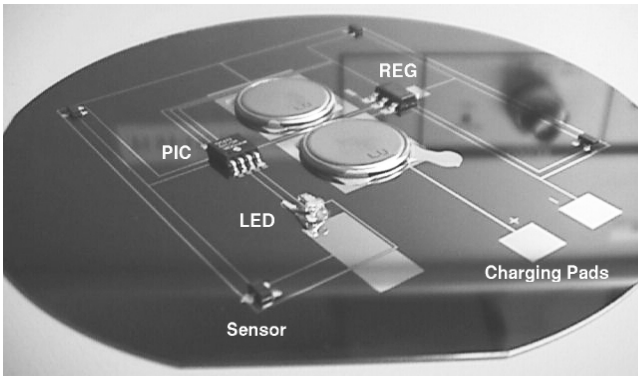

Figure 1: 4-station temperature sensor wafer.

MEMS techniques can be used to create a microfabricated "vacuum chamber" around the electronics so that thermal conduction and convection are virtually eliminated[15].

3 Component-Based Approach

Employing commercially available surface mount components, we have fabricated a 4-station temperature sensor wafer, capable of autonomous operation. The sensor wafer is intended for use in plasma-etch chambers, where temperatures do not exceed $60°C$. Operation at higher temperatures is primarily limited by potential out-gasing of the batteries. The design features a microprocessor, battery power, and infrared communications (see Figure 1). Components on the wafer surface protrude upward a maximum of 1.6 mm, which is sufficiently within the clearance provided by the robotics of most plasma etchers.

Temperature is sensed using precision integrated-circuit temperature sensors (LM61B) manufactured by National Semiconductor. These are 3-pin devices that output a voltage proportional to temperature. The output from each is fed to the A/D channels of the microprocessor. The microprocessor is a PIC12C672 manufactured by Microchip[1]. A Burr-Brown 2.85 V low-dropout voltage regulator (REG1117A) is used to ensure reliable operation of the microprocessor.

We use a digital output on the microprocessor to directly drive the infrared LED. The LED accounts for most of the power consumption of the wafer, drawing on average 1 mA. An Aluminum pad is placed below the LED to improve efficiency. The LED has a range of roughly 40 cm, which is sufficient to reach a receiver mounted on the view-port outside the plasma chamber.

The batteries are standard 3 V Lithium-ion cells (CR 1616) manufactured by Renata[2], with a capacity of 50 mAh. We use two of these cells in series to produce a voltage high-enough to power the regulator for a sufficient length of time. Future designs may be based on new *ultra-thin* (500 μm) battery-cell technology under development at Panasonic[3] for smart cards. Along with flip-chip IC components, these batteries would enable low profile component-based designs.

The wafer itself was fabricated in a single mask process, to pattern a layer of Aluminum interconnect over a thermally grown oxide. Processing was performed in the Berkeley Microlab. Components were attached to the Aluminum pads using conductive silver paint. This method was chosen in favor of thermal methods, as the high-thermal conductivity of silicon procludes the use of most conventional soldering methods. The resulting contacts are satisfactory, with silver paint having a resistivity of approximately 0.5 Ω/cm.

An HSDL-7000 from Hewlett-Packard is used on the receiving end to convert the infrared signal into an RS232 compatible format that can be fed into the serial port of a PC. The serial port is then read on the PC, and the data is graphically displayed on the screen and/or saved to a data file for inspection. The infrared data signal conforms with standard IrDA connectionless protocol operating in broadcast mode. Standard CRC-CCITT based error detection is implemented.

At present, we are exploring passivization techniques to enable operation of the wafer within a plasma chamber. As discussed in the sensor design issues section of this paper, there are many types of isolation that must be addressed. Simultaneously, the wafer will be tested and calibrated on an adjustable, precison bake-plate.

4 Fully-Integrated Approach

While the use of off-the-shelf components for sensor-wafer construction will work for several applications, many applications require a more integrated approach. For example, to thermally protect components for use in rapid thermal processing (RTP), only MEMS-based vacuum chamber isolation techniques offer adequate thermal isolation for this high temperature environment. Simply using off-the-shelf components and attempting to cover them with thermal shielding clearly will not work. Also, in some applications, the solder or silver paste used to connect components together in the off-the-shelf method can cause severe contamination problems. In these cases, using flip-chip bonded IC chips is one of the only ways to go.

[1] `http://www.microchip.com`

[2] `http://www.netbox.com/powersource/renata.html`

[3] `http://www.mbi.panasonic.co.jp/english/pi/news_e/980903_1e.html`

To create a fully-integrated wafer, one option would be to simply fabricate the entire wafer using a CMOS or equivalent process. While this could definitely produce several useful sensor and interconnection structures, this method would be prohibitively expensive for large substrates. And if this sensor wafer is to be used in the development of new equipment, a full process might not exist for the wafer size being used. Therefore, alternative methods for creating a fully-integrated sensor wafer must be utilized. One such method would be to use a blank substrate wafer with minimal low-resolution patterning to create a metal interconnection grid. This grid would then have positions set aside for separate sensor dice, created using a more established process. These dice would then be bonded to the base-wafer, using the base-wafer's metal lines to interconnect dice. This method not only allows the much more economical fabrication of a sensor wafer, but offers several advantages as well. Since the dice are added to the wafer individually, the metal interconnections can be made generic, so that several different types of sensor can be added to the wafer to suit the process being monitored. Also, the power and communications electronics can be fabricated to mate to the standard interconnections, so that these, too, can be placed in advantageous locations.

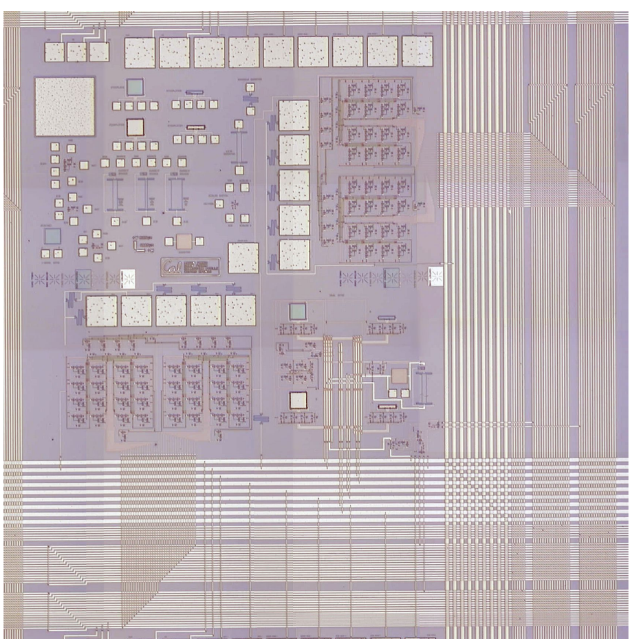

Figure 2: Photograph of fully-integrated *in-situ* etch-rate sensor wafer

Overall, the fully-integrated approach offers several advantages over the off-the-shelf methodology. However, due to its added complexity, this method requires much more development time. Therefore, this is a more long-term goal, while the off-the-shelf method offers a quick-turnaround approach for designing power, communication, and sensor technologies independently.

For the purpose of testing the concepts described above, a prototype sensor wafer was designed and fabricated. This wafer contains 57 sets of fully interconnected etch-rate sensors, with on-board sensor drive and switching electronics. Each "set" of sensors includes four different geometries of van der Pauw structures, which are designed to electrically measure film-thickness. The sensor wafer was fabricated using the Berkeley CMOS Baseline process, which is a 12 mask, double-poly, twin-well $1.3\mu m$ CMOS process. See Figure 2 for a photograph of a $1cm^2$ area of the finished wafer. Preliminary testing of this film-thickness transduction scheme shows promising results. Figure 3 shows the output from three of the sensors during a XeF_2 etch cycle. Because the etch-rate of the XeF_2 etchant used was very high due to the low exposed-area, gauge analysis could not be performed. The sensors were etched completely away in the span of a few seconds.

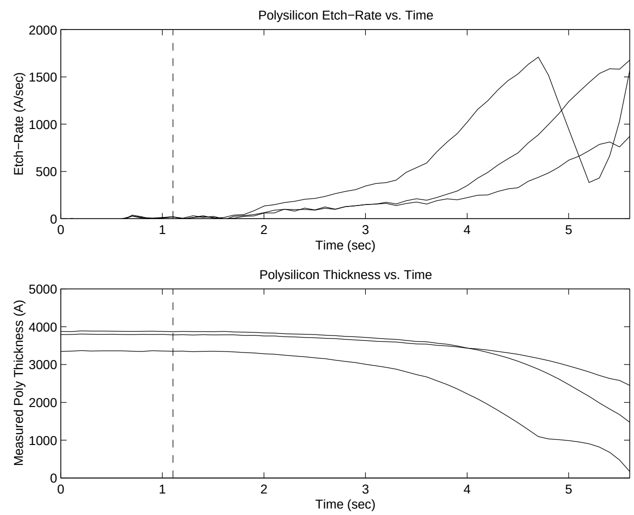

Figure 3: Experimental data from three sensors during a XeF_2 etch process

To correct this high etch-rate problem, a new sensor wafer was designed and fabricated. This wafer includes a polysilicon "guard-ring" around the wafer periphery to reduce the etch rate by "loading" the XeF_2 etcher. In addition, a simple two-mask process was used to fabricate the wafer, reducing the turn-around time to just under two weeks. Because of the simplicity of the process, however, no onboard electronics were used, and all multiplexing and amplification occurs externally.

An experiment was performed in which this sensor wafer was repeatedly etched for a short period of time and then measured using reflectometry to gauge the actual sensor film thickness. The sensor output during one of the etch cycles is shown in Figure 4. Due to the high selectivity of XeF_2 to SiO_2 , the thin native oxide on the polysilicon causes high surface roughness (∼1000 Å) in the etched films. Therefore, the reflectometry measurements taken between etch cycles cease to be accurate once the film begins to be etched. For this reason, no sensor calibration could be performed. Another problem experienced during this experiment was the temperature-sensitivity of the polysilicon resistivity. Because the XeF_2 - Si reaction is highly exothermic, once the oxide breaks through on the edge of the wafer and the silicon begins to be etched, the temperature of the entire wafer goes up by about 10-20 °C. Because heavily doped semiconductors exhibit an increase in resistivity with increasing temperature due to the decreasing carrier mobility[19], this increase in wafer temperature can manifest itself as an apparent loss of thickness. This was observed in one of the etch cycles (see Figure 5), in which the native oxide layer was still present. During this cycle no loss in thickness occured, yet a dip in sensor output was observed due to remote wafer heating. A new design is currently being fabricated that will alleviate the problems experienced during this experiment.

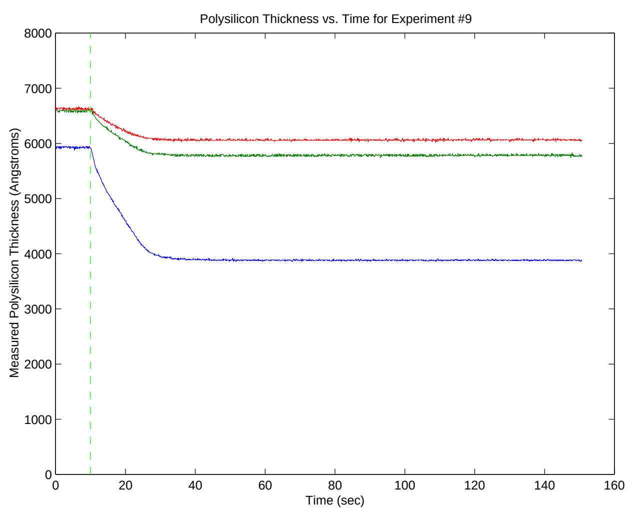

Figure 4: Experimental data from three sensors during XeF_2 etch cycle

5 Conclusions

In this paper we have described our on-going development of micro-sensor arrays for use in semiconductor manufacturing. These sensor arrays are autonomous *vis-a-vis* power and communications, and are passivated to withstand modestly harsh environments. We submit that these on-wafer arrays of sensors offer unprecedented process and wafer measurement capability at modest capital cost. Our preliminary approaches to developing these sensor arrays are two-fold: component based designs and fully-integrated designs. A number of difficult technical issues including effective environmental isolation, ease of manufacturability, and calibration need to be resolved before our vision comes to fruition.

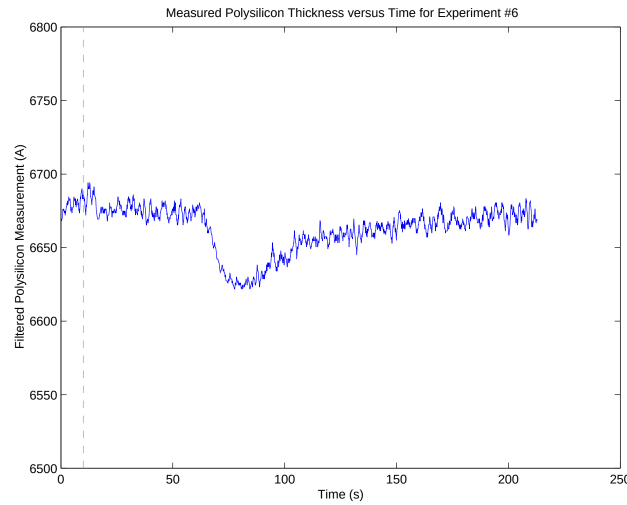

Figure 5: Experimental data from a single sensor, showing dip in thickness due to temperature rise

References

[1] H. Durakpasa, M.W. Breiter and B. Dunn, "Impedance Studies of Sol-Gel Materials," *Electrochim. Acta*, vol. 38, 371, 1993.

[2] B. Dunn, G.C. Farrington and B. Katz, "Sol-Gel Approaches for Solid Electrolytes and Electrode Materials," *Solid State Ionics*, vol. 70, 3, 1994.

[3] F. Chaput, B. Dunn, P. Fuqua and K. Salloux, "Synthesis and Characterization of Vanadium Oxide Aerogels," *J. Non-Crystalline Solids*, vol. 188, 11, 1995.

[4] K. Salloux, F. Chaput, H.P. Wong, B. Dunn and M.W. Breiter, "Lithium Intercalation in Vanadium Pentoxide Aerogels," J. Electrochemical Society, 142, L 191 (1995).

[5] B.C. Dave, B. Dunn, F. Leroux, L.F. Nazar and H.P. Wong, "Vanadium Oxide/Polypyrrole Aerogel Nanocomposites," *Mat. Res.Soc.Symp.Proc.*, 435, 611, 1996.

[6] W. Liu, G.C. Farrington, F. Chaput and B. Dunn, "Synthesis and Electrochemical Studies of Spinel Phase $LiMn_2O_4$ Cathode Materials Prepared by the Pechini Process," *J. Electrochem. Soc.*, vol. 143, 879, 1996.

[7] P-W. Wu, S.R Holm, A.T. Duong, B. Dunn and R.B. Kaner, "A Sol-Gel Solid Electrolyte with High Lithium Ion Conductivity," *Chem. Mater.*,vol. 9, 1004, 1997.

[8] "Thin-film rechargeable lithium batteries," John Bates, Oak Ridge National Laboratory.

[9] B. Gerold *et al.*, Sematech APC, Sept. 1997, Lake Tahoe, Nevada.

[10] Xiaohua Yu, J.B. Bates, G.E. Jellison, Jr., and F.X. Hart, "A stable Thin-Film Lithium Electrolyte: Lithium Phosphorus Oxynitride," *J. Electrochem. Soc.*, Vol 144, No. 2, February 1997.

[11] B. Wang, J.B. Bates, F.X. Hart, B.C. Sales, R.A. Zuhr, and J.D. Robertson, "Characterization of Thin-Film Rechargeable Lithium Batteries with Lithium Cobalt Oxide Cathodes," *J. Electrochem. Soc.,* Vol 143, No. 10, October 1996

[12] John Vig, Raymond L. Filler, and Yoonkee Kim, "Uncooled IR Imaging Array Based on Quartz Microresonators," *J. Microelectromechanical Systems,* Vol. 5, No. 2, June 1996.

[13] Jeong B. Lee, Zhizhang Chen, Mark G. Allen, Ajeet Rohatgi, and Rajeewa Arya, "A Miniaturized High-Voltage Solar Cell Array as an Electrostatic MEMS Power Supply," *J. Microelectromechanical Systems,* Vol. 4, No. 3, September 1995.

[14] Kurt E. Petersen, "Silicon as a Mechanical Material," *Proceedings of the IEEE,* Vol. 70, No. 5, May, 1982.

[15] Kovacs, Gregory T.A., Micromachined Transducers Sourcebook, pp. 586-587, (1998).

[16] Devi Gunawan, Lih-Yuan Lin, Kristofer J. Pister, "Micromachined corner-cube reflectors as a communication link," *Sensors and Actuators*, 46-47, pp: 580-583, 1995.

[17] G.W. Marsh and J.M. Kahn, "Channel Reuse Strategies for Indoor Infrared Wireless Communications," *IEEE Trans. on Commun.,* vol. 45, no. 10, pp. 1280-1290, October, 1997.

[18] A.P. Tang, J.M. Kahn and K.P. Ho, "Wireless Infrared Communication Links using Multi-Beam Transmitters and Imaging Receivers," *IEEE Intl. Conf. on Commun.*, pp. 180-186, Dallas, Texas, June 23-27, 1996.

[19] Jacob Millman and Christos C. Halkias, Integrated Electronics, pp. 1-18, (1972).